78P2241B
E3/DS3/STS-1
Line Interface Unit

DATA SHEET

JULY 2005

DESCRIPTION

The 78P2241B is a line interface transceiver IC for E3, DS3, STS-1, NA T3 and ATM applications. It includes clock recovery and transmitter pulse shaping functions for applications using 75-ohm coaxial cable at distances up to 1100 feet. These applications include DSLAMs, digital multiplexers, SONET Add/Drop multiplexers, PDH equipment, DS3 to Fiber optic and microwave modems and ATM WAN access for routers and switches.

The receiver recovers clock and data from a B3ZS or HDB3 coded AMI signal. It can compensate for over 12dB of cable and 6dB of flat loss. The transmitter generates a signal that meets the standard pulse shape requirements.

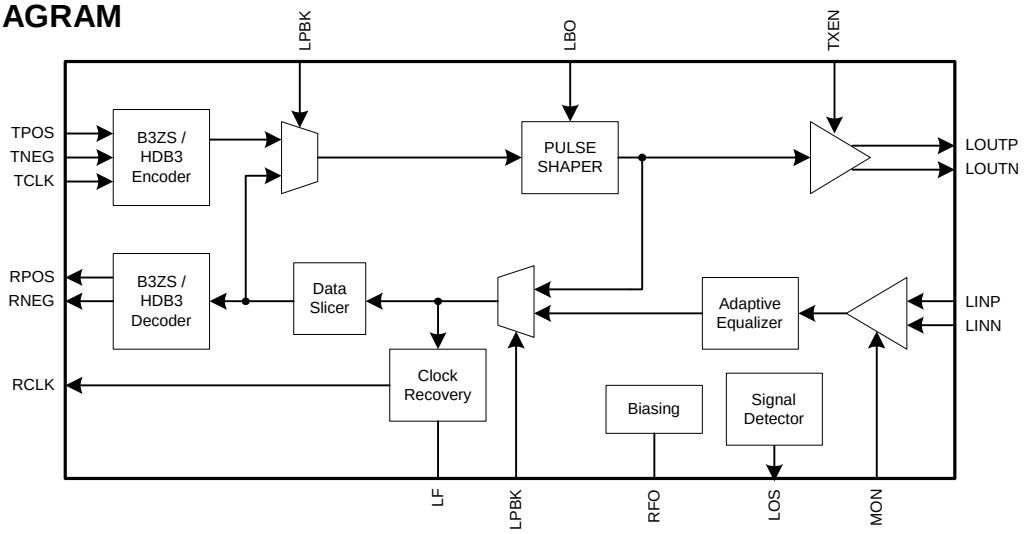
The 28-pin PLCC 78P2241B is pin and functionally compatible to the 78P7200L and the 78P2241 (28 PLCC version). The 78P2241B in the 48-pin TQFP is pin compatible with the 78P2241 in the same package. To the 78P7200L functionality, it adds a B3ZS/HDB3 ENDEC, line code violation detector, loop-back and clock polarity selection as well as ability to receive a DSX3 monitor signal. The line code violation detector has been added to the 78P2241 functionality.

The 78P2241B is manufactured in an advanced BICMOS process and operates at both 5V and 3.3 V power supply voltages. It consumes less than 110 mA of supply current.

FEATURES

- **Single chip transmit and receive interface for E3, DS3 and STS-1 applications.**
- **Interface to 75 ohm coaxial cable over 1100 feet at speeds up to 51.84 Mbps.**
- **Compliant with ANSI T1.102-1993, Telcordia GR-499-CORE and GR-253-CORE, ITU-T G.703, G.823 for jitter tolerance, and G.775 for loss of signal.**
- **Compliant with ATM FORUM af-phy-0034 (E3 public UNI) and af-phy-0054 (DS3 public UNI).**
- **Easily Interfaced to ATM framer ICs such as PMC 7345 , 7346 QJET and 7321.**
- **Unique clock recovery requires no reference clock or crystal oscillator.**
- **Receive DS3-high and DSX3 monitor signals**
- **Includes diagnostic loop-back for AMI and digital signals.**
- **Includes a selectable B3ZS/HDB3 ENDEC.**
- **Pin compatible to 78P7200 (28-lead PLCC) and 78P2241.**
- **28-lead PLCC and 48-lead TQFP packages**
- **3.3 or 5 V operation, ICC<110mA**
- **Input circuit works either Transformer or Capacitor coupled**
- **Line-code violation detector**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The 78P2241B is a single chip line interface IC designed to work with a 51.84 Mbit/s STS-1, 44.736 Mbit/s DS3 or 34.368 Mbit/s E3 signal. The receiver recovers clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal. The AMI line input signal should be B3ZS or HDB3 coded.

The transmitter accepts clock, positive, and negative data and converts them into an AMI signal to drive a 75Ω coaxial cable. The shape of the transmitted signal though any cable length of 0 to 450 feet complies with the published templates of ANSI T1.102-1993, Telcordia TR-NWT-000499 and GR-253-CORE, ITU-T G.703. The 78P2241B is designed to work with B3ZS or HDB3 coded signals. The B3ZS or HDB3 encoding and decoding functions are normally included in the framer ICs; however, a selectable B3ZS/HDB3 ENDEC is included in the 78P2241B for interface to binary NRZ data. The 78P2241B is designed to easily connect to popular ATM framer ICs such as PMC 7345 (SUNI-PDH), PMC 7346 (QJET) and 7321.

OPERATION SPEED

Internal bias generators that are adjusted by the value of the RFO set the 78P2241B PLL center frequency and Transmitter amplitude for the different standards. The E# pin controls the equalizer response and the transmitter pulse shape and amplitude. The following table shows the proper settings.

Standard	RFO Value, kΩ	E# pin setting
E3	6.81	Low
DS3	5.23	High
STS-1	4.53	Float

RECEIVER

The receiver input can be either transformer-coupled or capacitor coupled to the AMI signal. In applications where the highest performance and isolation is required, a 1:1 transformer is used on the receiver path. In the applications, where isolation is provided elsewhere in the circuit, an AC coupling can be used. The inputs to the IC are internally referenced to Vcc. Since the input impedance of the 78P2241B is high, the AMI line must be terminated to 75Ω. The input signal of the 78P2241B must be limited to a maximum of three consecutive zeros using a coding scheme such as B3ZS or HDB3.

The AMI signal first enters a selectable fixed 20 dB amplifier stage that compensates for very low amplitude DSX3 monitor signal when MON pin is held high. The signal then enters an equalizer and AGC gain stage. The equalizer is designed to overcome intersymbol interference caused by long cable lengths. Because the equalizer is adaptive, the circuit will work with all square shaped signals such as DS3 high or 34 Mbit/s E3. The variable gain differential amplifier maintains a constant voltage level output regardless of the input voltage level. The gain of the amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a phase locked loop with an auxiliary frequency-sensitive acquisition loop. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for an external, high precision tuned circuits or reference clock signal.

The jitter tolerance of the 78P2241B meets the requirements of Telcordia GR-499-CORE for Category I equipment for DS3 rates and exceeds the requirements of ITU-T G.823 for E3 rates.

Pin 21 MON	Receive Range mVpk	Mode
Low	90-850	DS3/STS-1 normal
High	25-80	DS3 monitor
Low	104-1200	E3 normal
High	25-80	E3 monitor

B3ZS/HDB3 DECODER

The 78P2241B includes a selectable B3ZS/HDB3 Encoder/Decoder (ENDEC). When the ENDEC pin is low, the ENDEC is selected and the receiver generates a composite NRZ logic data following the B3ZS (for DS3/STS-1) or HDB3 (for E3) substitution codes via the RPOS/RNRZ pin as shown below.

Pin 20 ENDEC	RPOS/RNRZ	RNEG
High	Positive AMI	Negative AMI
Low	NRZ data	No Connect

FUNCTIONAL DESCRIPTION (continued)

The decoder also detects Receive Line Code Violations (RLCV) and outputs a pulse via the RNEG/RLCV pin. Three different classes of line code violations are detected.

1) Too many zeros: More than two (three) consecutive zeros in B3ZS (HDB3) mode.
2) Not enough zeros between bipolar pulse (B) and bipolar violation pulse (V): (B,V) for B3ZS, (B,V) or (B,0,V) for HDB3.
3) Code violation: Even number of bipolar pulses (B) detected between bipolar violation pulses (V).

On the transmit side, NRZ input data is internally converted to Positive and Negative logic data following the B3ZS (for DS3/STS-1) or HDB3 (for E3) substitution codes. The NRZ data is input to the TPOS/TNRZ pin as shown below.

Pin 20 ENDEC	TPOS/TNRZ	TNEG
High	Positive AMI	Negative AMI
Low	NRZ data	LCV

LOSS OF SIGNAL

Should the input signal fall below a minimum value for 175 +/- 75 cycles of the receive clock RCLK, the loss of signal indication, LOS goes low. LOS goes high when a valid signal is received at the input for at least 175 +/- 75 cycles of the receive clock.

TRANSMITTER

The transmitter accepts logic level clock (TCLK), positive data (TPOS) and negative data (TNEG) signals and generates current pulses on the LOUT+ and LOUT- pins. When properly connected to a center-tapped 1:2 transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable.

When the recommended transformer is used and the E# pin is set high, the transmitted pulse shape at the end of the 75Ω terminated cable of 0 to 450 feet will fit the DS3 template in ANSI T1.102-1993 and Telcordia GR-499-CORE standard documents.

For STS-1 applications, the transmitted pulse for a short cable meets the requirements of Telcordia GR-253-CORE. The E# pin should be allowed to float.

For E3 applications, the transmitted pulse for a short cable meets the requirements of ITU-T G.703. The E# pin is to be pulled low.

RCLK/TCLK polarity reversal:

To simplify the interface with framer circuitry, RCLK and TCLK can be inverted with the ICKP pin.

Pin 10 ICKP	RCLK	TCLK
Low	Normal	Normal
Float	Invert	Invert
High	Normal	Invert

Loop-back modes:

The following loop-back modes allow for the diagnostic test of the PC board. This function is controlled by the LPBK pin.

Pin 28 LPBK	Loop-back
Low	Local loop-back (LLB)
Float	Remote loop-back (RLB)
High	Normal Operation

Local loop-back:

When LPBK is low, the 78P2241B enters Local loopback. In this mode, the LOUT+/- transmit signals are internally routed to the receiver input circuit. The incoming line receiver AMI signal on LIN+/- is ignored. With the transmitter still tied to the cable, this test mode can indicate a short circuit on the transmitter external components or other problem in the transmit path.

Remote loop-back:

When LPBK pin is allowed to float, the 78P2241B enters remote loopback mode. The RPOS/RNEG and RCLK pins are internally tied to the TPOS/TNEG and TCLK so the same AMI signal that is received by the framer is transmitted back to the far end where a bit continuity test can be performed.

Line Build-Out:

The Line Build-Out function controls the amplitude in DS3 and STS-1 mode. The selection of LBO depends on the amount of cable the transmitter is connected to. When used with less than 225 ft of cable the LBO pin should be pulled high. With 225ft or more cable the LBO pin should be low.

PIN DESCRIPTION: (The 28-pin PLCC is compatible with 78P7200)

NAME	PIN TQFP	PIN PLCC	TYPE	DESCRIPTION
LIN+ LIN-	42 44	1 3	I	Line Input: Differential AMI inputs to the chip. Should be transformer coupled and terminated at 75-ohm resistor.
RCLK	33	23	O	Receive Clock: Recovered receive clock.
RPOS/ RNRZ	35	25	O	Receive Positive Data / NRZ Data: When ENDEC is high, this pin indicates reception of a positive AMI pulse on the coax cable. When ENDEC is low, it outputs NRZ data.
RNEG/ LCV	34	24	O	Receive Negative Data/LCV: When ENDEC is high, this pin indicates reception of a negative AMI pulse on the coax. When ENDEC is low this pin indicates the occurrence of a line code violation.
LOS	39	27	O	Loss of Signal: logic low indicates that receiver signal (LIN±) is below the threshold level for 175±75 periods. RPOS and RNEG are forced low when LOS=0.
LOUT+ LOUT-	9 11	9 11	O	Line Out: Differential AMI Output. Requires a 2:1 center tapped transformer and 301Ω resistor.
TCLK	18	16	I	Transmitter Clock Input: This signal is used to latch the TPOS/TNRZ and TNEG signals into the 78P2241.
TPOS/ TNRZ	16	14	I	Transmit Positive Data / Transmit NRZ: When ENDEC is high, a logic one on this pin generates a positive AMI pulse on the coax. This pin should not be high at the same time that TNEG is high. When ENDEC is low, NRZ data received on this pin is encoded into positive and negative AMI pulses.
TNEG	17	15	I	Transmit Negative Data: When ENDEC is high, a logic one on this pin generates a negative AMI pulse on the coax. This pin should not be high at the same time that TPOS/TNRZ is high. When ENDEC is low, this pin is ignored.
LBO	13	12	I	Line Build-Out, Transmitter: Logic low used with 225ft or more of cable is used on transmit path. Logic high used with less than 225ft of cable.
E#	15	13	I3	DS3, E3 and STS-1 Select: Set low for E# applications. Set high for DS3, allow to float for STS-1 operation. Formerly OPT! On the 78P7200.
TXEN	22	18	I	Transmitter Enable: When high, enables transmitter. When low, tri-states transmitter drivers, LOUT±. This pin was called OPT@ on 78P7200.
MON	28	21	I	DSX3 / E3 Monitor Select: When set high, an additional 20-dB gain stage is added to the receiver gain. This pin was tied to GND on the 78P7200.
ICKP	10	10	I3	Invert Clock Polarity: When low, the polarities of RCLK and TCLK are the same as those on the 78P7200. When set high, the polarity of TCLK is inverted. When allowed to float, the polarities of both RCLK and TCLK are inverted.
LPBK	40	28	I3	Loop-back Select: When high, neither loop-back is activated. When allowed to float RPOS, RNEG and RCLK are looped back onto TPOS, TNEG and TCLK. When low, LOUT± is looped back onto LIN±.
VCC	5,6,20, 21,37,38	7,17,26	P	Power Supply.

PIN DESCRIPTION: The 28-pin PLCC is compatible with 78P7200 (continued)

NAME	PIN TQFP	PIN PLCC	TYPE	DESCRIPTION
GND	1, 3, 4, 7, 8, 12, 14, 19, 23, 24, 25, 29, 30, 31, 32, 36, 41, 43, 45, 46, 47, 48	2,4,6,8,22	P	Ground. Connecting all ground pins to a common ground plane is recommended.
RFO	2	5	-	A resistor to GND sets the operational speed of the chip. RFO= 5.23K for DS3, RFO=6.81K for E3 and RFO=4.53K for STS-1.
LF1	26	19	-	Receiver PLL filter capacitor.
ENDEC	27	20	I	Encoder/Decoder: When set low, activates B3ZS/HDB3 ENDEC on receiver and transmitter logic signals.

Note 1: Pin type: I-input; I3-three level logic input; O-output; P-power supply. Advanced Data sheet pin assignment and functions are subject to change.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond these maximums rating may permanently damage the device.

PARAMETER	RATING
Positive supply, V_{CC}	6V
Storage temperature	-65 to 150
Ambient operating temperature	-40 to +85 °C
Output Pin Voltage (LOUT+, LOUT-) Input Pin Voltage (LIN+, LIN-)	V_{CC} –2 to V_{CC} +2 V
Input pin voltage, all other pins	V_{CC}+0.3 to GND-0.3 V

DC CHARACTERISTICS: Ta = -40° to +85°C; positive supply voltage = 5V ±0.5V or 3.3V±0.3V

PARAMETER	PIN TYPE	CONDITION	MIN	TYP	MAX	UNIT
Supply current I_{CC}		Transmit and receive all ones, VCC=5V or 3.3V		70	110	mA
Supply current I_{CC}		transmitter disabled, TXEN=0		35		mA
V_{IL}	I				0.8	V
V_{IH}	I		2			V
I_{IL}, I_{IH}	I		-10		+10	µA
V_{IL3}	I3				0.5	V
Z_{IM3}	I3	Input Floating	8	10	20	kΩ
V_{IH3}	I3		V_{CC}-0.5			V
I_{IL3}, I_{IH3}	I3		-100		+100	µA
V_{OL}	O	I_{OL}=-0.1mA			0.5	V
V_{OH}	O	I_{OL}=+0.1mA	V_{CC}-0.5			V

E3 – RECEIVER (RFO = 6.81kΩ, E# is set low), receiver is transformer-coupled.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Peak Differential Input Amplitude, LIN+, LIN-	See Note 2	104		1200	mV_{pk}
Peak Differential Input Amplitude, LIN+, LIN- Monitor Mode	MON=1	25.5		85	mV_{pk}
Bit Error Ratio in the presence of an Interfering Signal at Receive Input	Interfering signal power 20dB below E3 signal power. Both are PRBS23 (2^{23}-1) patterns.		10^{-9}		
RCLK rise/fall time *TRCT*		2		4	ns
RCLK period, *TRCF*			29.10		ns
RCLK clock duty cycle		45		55	%
RCLK pulse width *TRC*			14.55		ns
RPOS/RNEG data setup time *TRDPS*	CL=15 pF	7			ns
RPOS/RNEG data hold time *TRDPH*	CL=15 pF	7			

Note 2: 104 mV_{pk} equals 950 mVP at the source with 1100 feet of cable (13.2dB loss).

Note 3: Meets the jitter tolerance requirement of ITU-T G.823.

Note 4: Measure the jitter's 3dB fall off on RCLK. In order to meet jitter transfer function requirements with a lower bandwidth, an external jitter attenuation circuit needs to be added.

DS3/STS-1 RECEIVER (RFO = 5.23kΩ for DS3 and 4.53kΩ for STS-1, E# pin is set high or allowed to float), Input is transformer coupled

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Peak Differential Input Amplitude, LIN+ and LIN- (see Note 5)	MON=0. Signal at DSX is 360-850mVP (see Note 6)	90		850	mVP
Peak Differential Input Amplitude, LIN+ and LIN-	Mon=1	25		80	mVP
Peak Differential Input Amplitude, LIN+ and LIN-	Mon=0. DS3 HIGH (see Note 7)	90		1200	mVP
Bit Error Ratio in the presence of an Interfering Signal (IS) at LIN+,LIN-	IS is a sinusoidal tone, 22.368 MHz for DS3 or 25.92MHz for STS-1. Data is a PRBS15 (2^{15}-1) pattern. IS power is 10dB below data signal power.		10^{-9}		
RCLK rise/fall time *TRCT*	CL=25pF		5		ns
RCLK period *TRCF*	DS3 STS-1		22.35 19.29		ns
RCLK pulse width *TRC*	DS3 STS-1		12.24 9.65		ns
RPOS/RNEG data setup time *TRDPS*	CL=15 pF	7			ns
RPOS/RNEG data hold time *TRPDH*	CL=15 pF	7			ns
LOS Threshold	Monitor Disabled		64		mVP
	Monitor Enabled		6.4		mVP

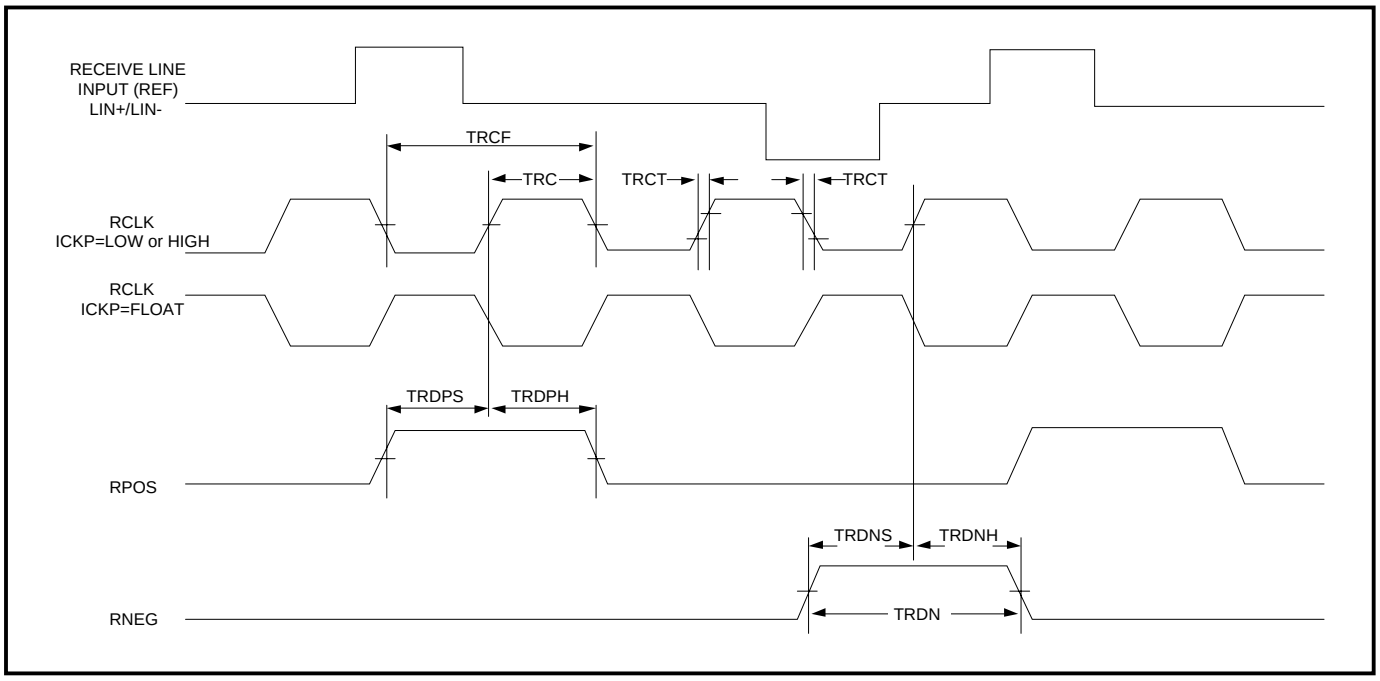
Note 5: Signal source should meet DS3 template of ANSI-T102.1993 Figure 4 and STS-1 template of ANSI-T102.1993 Figure 5, Loss characteristics of the WE728A or RG 59B cable should be better than Figure C2 of ANSI-T102.1993.

Note 6: Receiver can handle up to 450 feet of cable loss (5.5dB) from the DSX cross-connect.

Note 7: Case where test signal is fed directly into receiver with fast rise times violates DS3 template and normal maximum. In this mode no noise, jitter, or interfering tone impairments will be added.

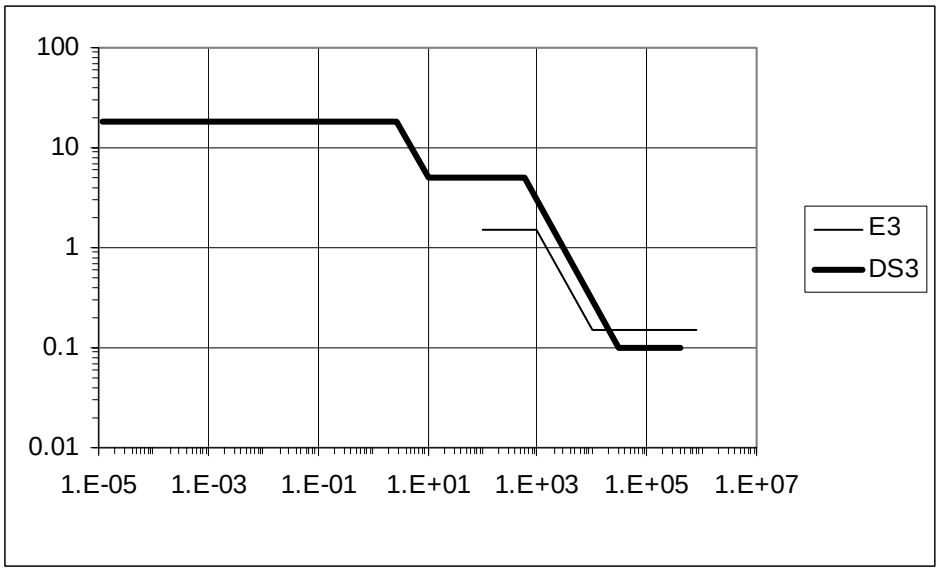
Note 8: This is performed in digital loop-back mode. Jitter is supplied by a Bit Error Rate Tester and bit errors are measured. Jitter is specified in terms of UI (Unit Interval) and frequency, is summed with DS3 PRBS15 data through 450 feet of cable.

TIMING DIAGRAM: Receive Waveforms (E3/DS3/STS-1)



RECEIVER JITTER TOLERANCE

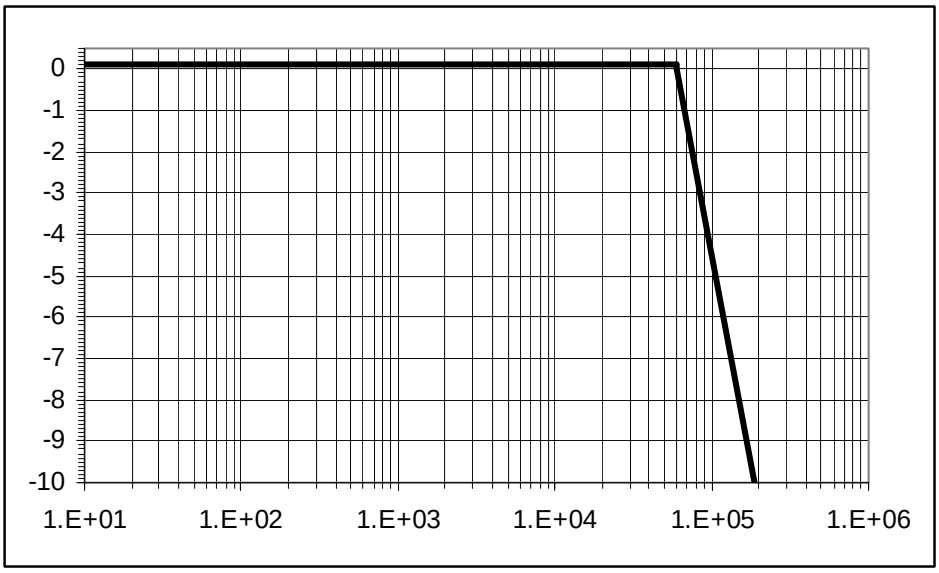
E3 and DS3 jitter tolerance specifications are in ITU-T G.823 and G.824. The E3 specification is the tighter of the two for frequencies greater than 20 kHz. Receive jitter tolerance is not tested during production test.



PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Receiver Jitter Tolerance	12μHz to 2.78 Hz 10Hz to 600Hz 20 kHz to 800 kHz	18 5 0.15			UI

RECEIVER JITTER TRANSFER FUNCTION

The receiver clock recovery loop filter characteristics are such that the receiver has the following transfer function. The corner frequency of the PLL is approximately 50 kHz. Receiver jitter transfer function is not tested during production test.



PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Receiver Jitter transfer function	below 59.6 kHz			0.1	dB
Jitter transfer function roll-off			20		dB/decade

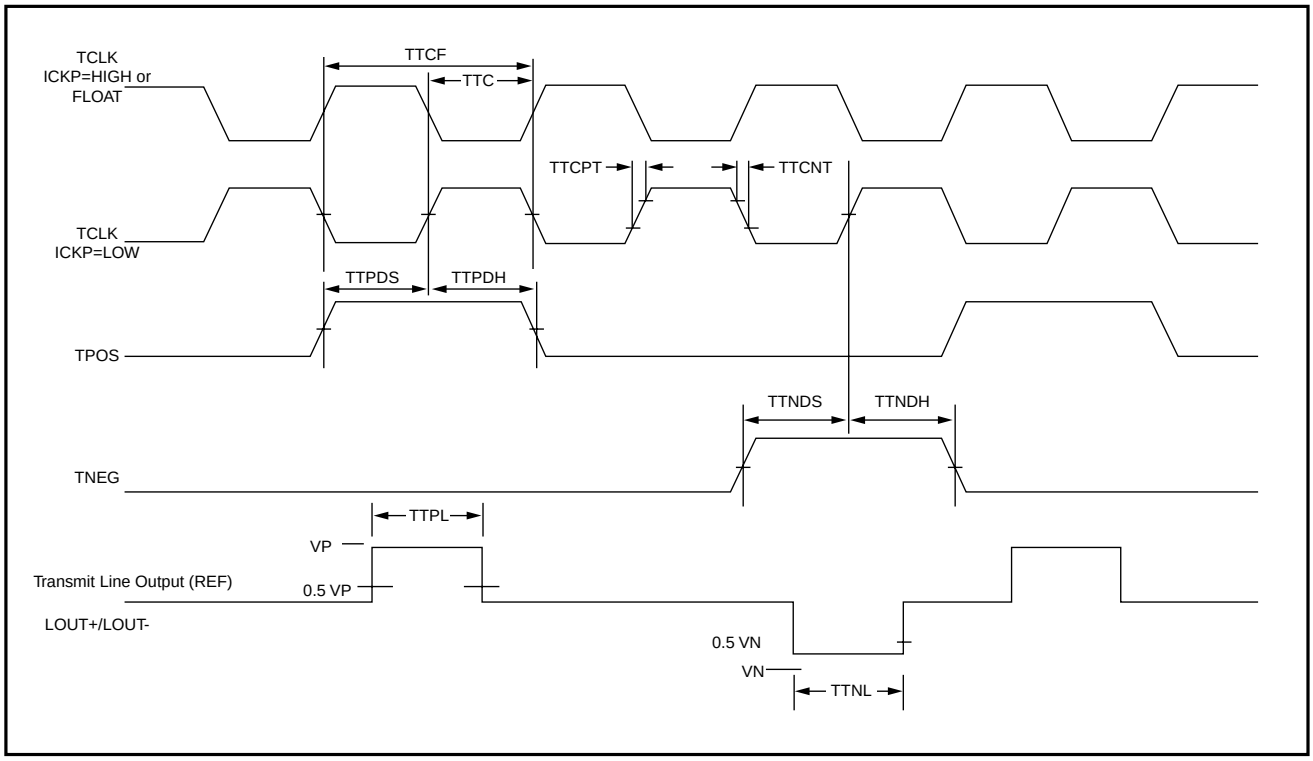
E3 – TRANSMITTER (RFO = 6.81kΩ, E# = LOW)

PARAMETER	CONDITION (see timing diagram)	MIN	TYP	MAX	UNIT
Transmitter amplitude	LOUT+ and LOUT-	900	1000	1100	mVP
Transmitter Amplitude Mismatch	Ratio of amplitudes of positive and negative pulses measured at pulse centers	0.95		1.05	
Transmitter width mismatch *TTPL/TTHL*	Ratio of widths of positive and negative pulses measured at pulse half amplitude	0.95		1.05	
Transmitter Pulse width TTPL, *TTPN*	LOUT+ and LOUT-		14.55		ns
Transmitter clock duty cycle, *TTC/TTCF*		40		60	%
Transmitter clock period *TTCF*			29.10		ns
Transmitter clock pulse width *, TTC*			14.55		ns
Transmitter clock transition time, Rising and falling *CPTT/CNTT*		0.8	3	5	ns
Data setup time *TTDRS*		2.5			ns
Data hold time *TTDHS*		2.5			ns

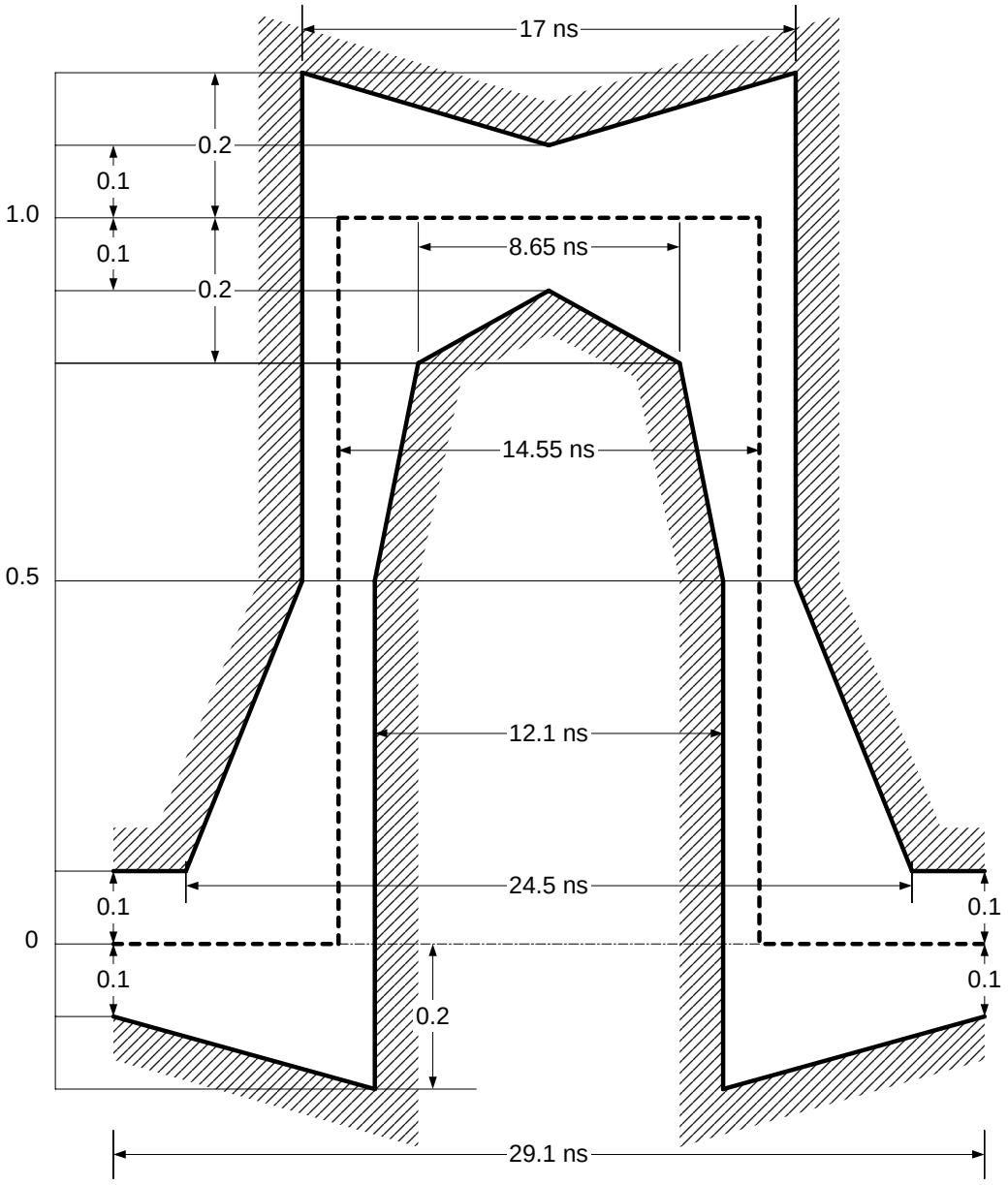
DS3/STS-1 TRANSMITTER (E# = High)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Transmitter Amplitude	LOUT+ and LOUT-	650	800	850	mVP
Transmit Amplitude with LBO on	LOUT+ and LOUT-	700		1300	mVP
Transmitter Amplitude Mismatch	Ratio of amplitudes of positive and negative pulses measured at pulse peaks.	0.9		1.1	
Transmitter power At 22.368 MHz	DS3 only - All ones, 3kHz bandwidth	-1.8		+5.7	dBm
Transmitter power At 44.736 MHz	DS3 only - All ones, 3kHz bandwidth	-21.8		-14.3	dBm
Transmitter clock duty cycle, *TTC/TTCF*		40		60	%
Transmitter clock period *TTCF*	DS3		22.35		ns
Transmitter clock period *TTCF*	STS-1		19.29		ns
Data setup time *TTPDS*		2.5			ns
Data hold time *TTPDH*		2.5			ns
Transmitter clock transition time, Rising and falling *TTCPT,TTCNT*		0.8	2	4	ns

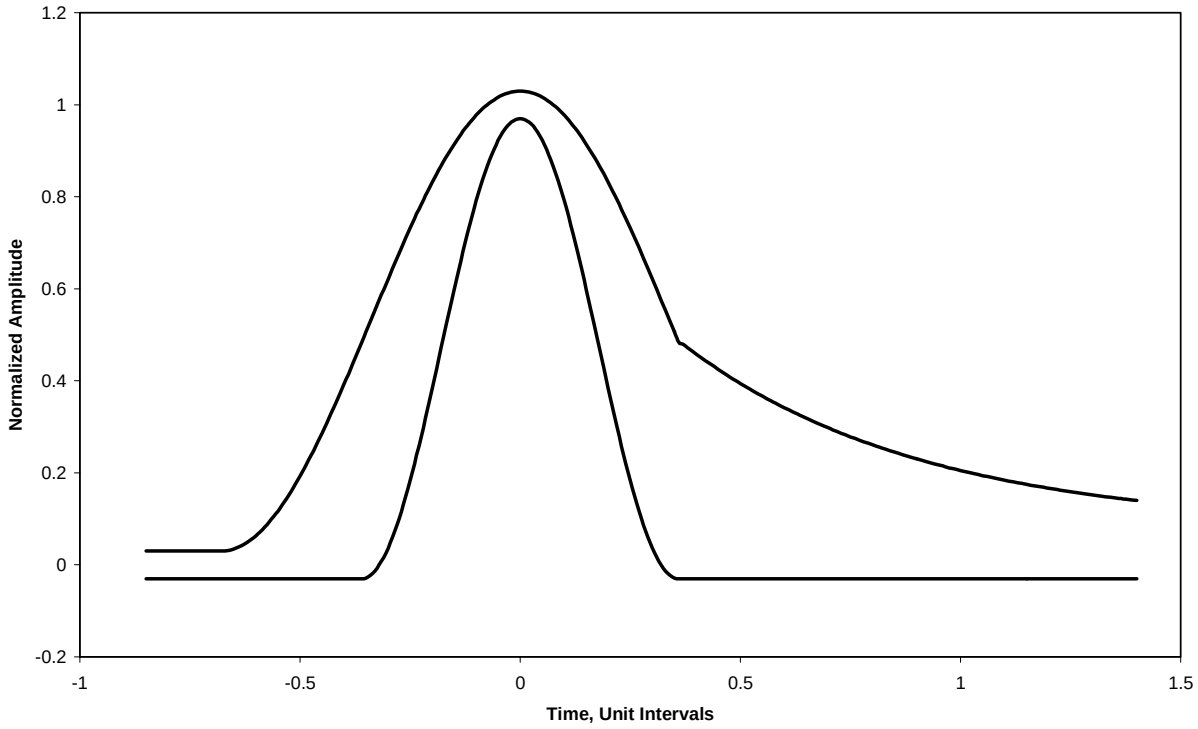
TIMINGING DIAGRAM: Transmitter Waveforms (E3/DS3/STS-1)



E3 TRANSMIT TEMPLATE

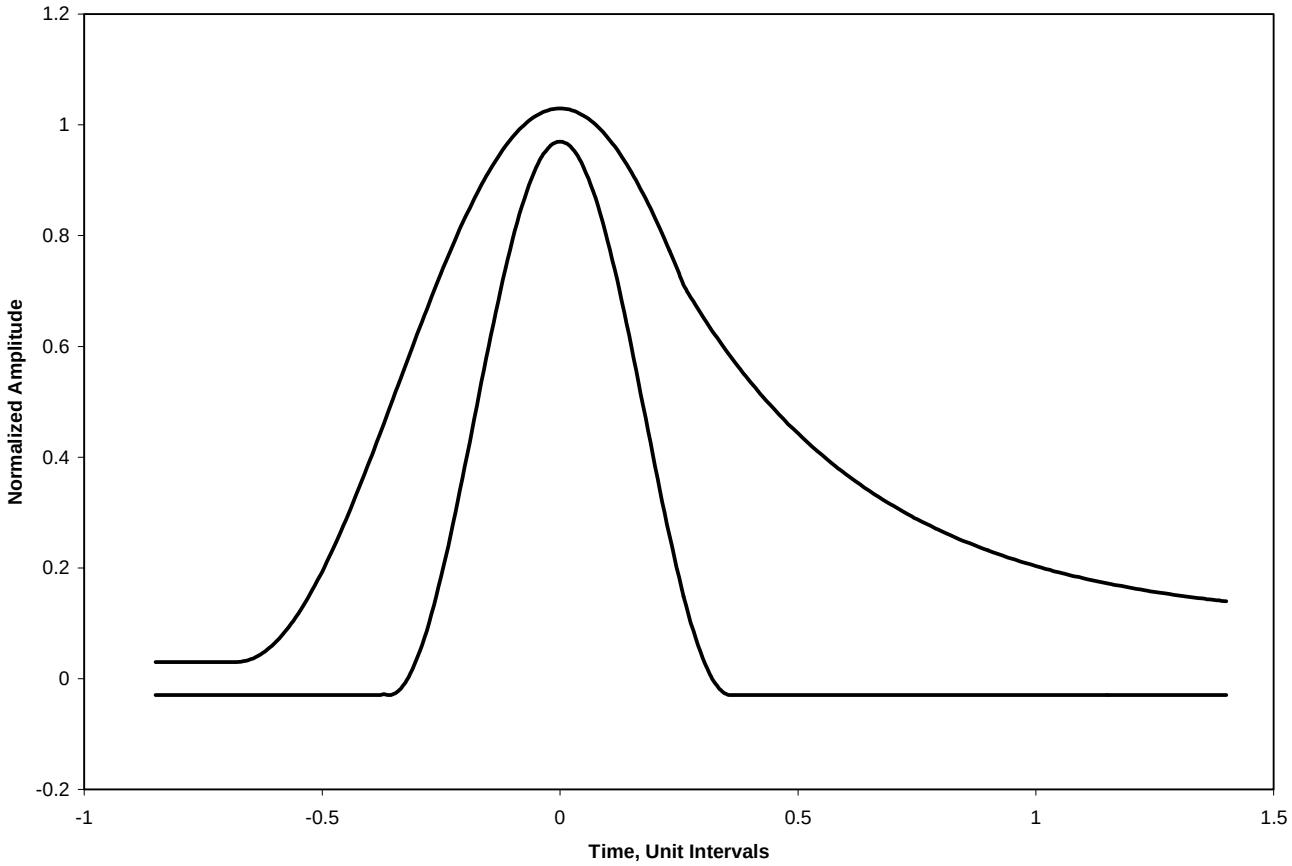


DS3 TRANSMIT PULSE TEMPLATE



Time axis range (UI)	Normalized amplitude equation
Upper Curve	
-0.85 ≤ T ≤ -0.68	0.03
-0.68 ≤ T ≤ 0.36	0.03 + 0.5{1+sin[(pi/2)(1+T/0.34)]}
0.36 ≤ T ≤ 1.4	$0.08+0.407\ e^{-1.84(T-0.36)}$
Lower Curve	
-0.85 ≤ T ≤ -0.36	-0.03
-.0.36 ≤ T ≤ 0.36	-0.03 + 0.5{1+sin[(pi/2)(1 + T/0.18)]}
0.36 ≤ T ≤ 1.4	-0.03

STS-1 TRANSMIT PULSE TEMPLATE

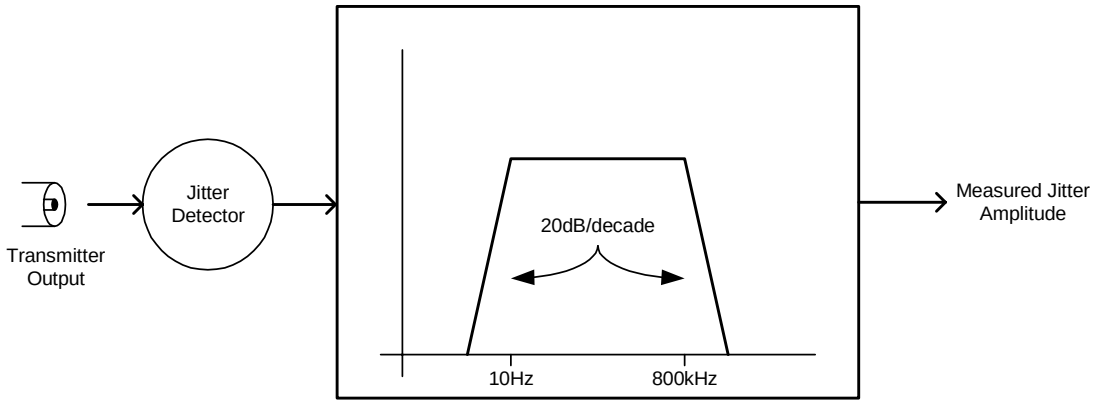


STS-1 (Transmit template specs)

Time axis range (T)	Normalized amplitude equation (A)
Upper Curve	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.03 + 0.5\{1+\sin[(\pi/2)(1+T/0.34)]\}$
$0.26 \leq T \leq 1.4$	$0.1+0.61\ e^{-2.4(T-0.26)}$
Lower Curve	
$-0.85 \leq T \leq -0.38$	-0.03
$-0.38 \leq T \leq 0.36$	$-0.03 + 0.5\{1+\sin[(\pi/2)(1 + T/0.18)]\}$
$0.36 \leq T \leq 1.4$	-0.03

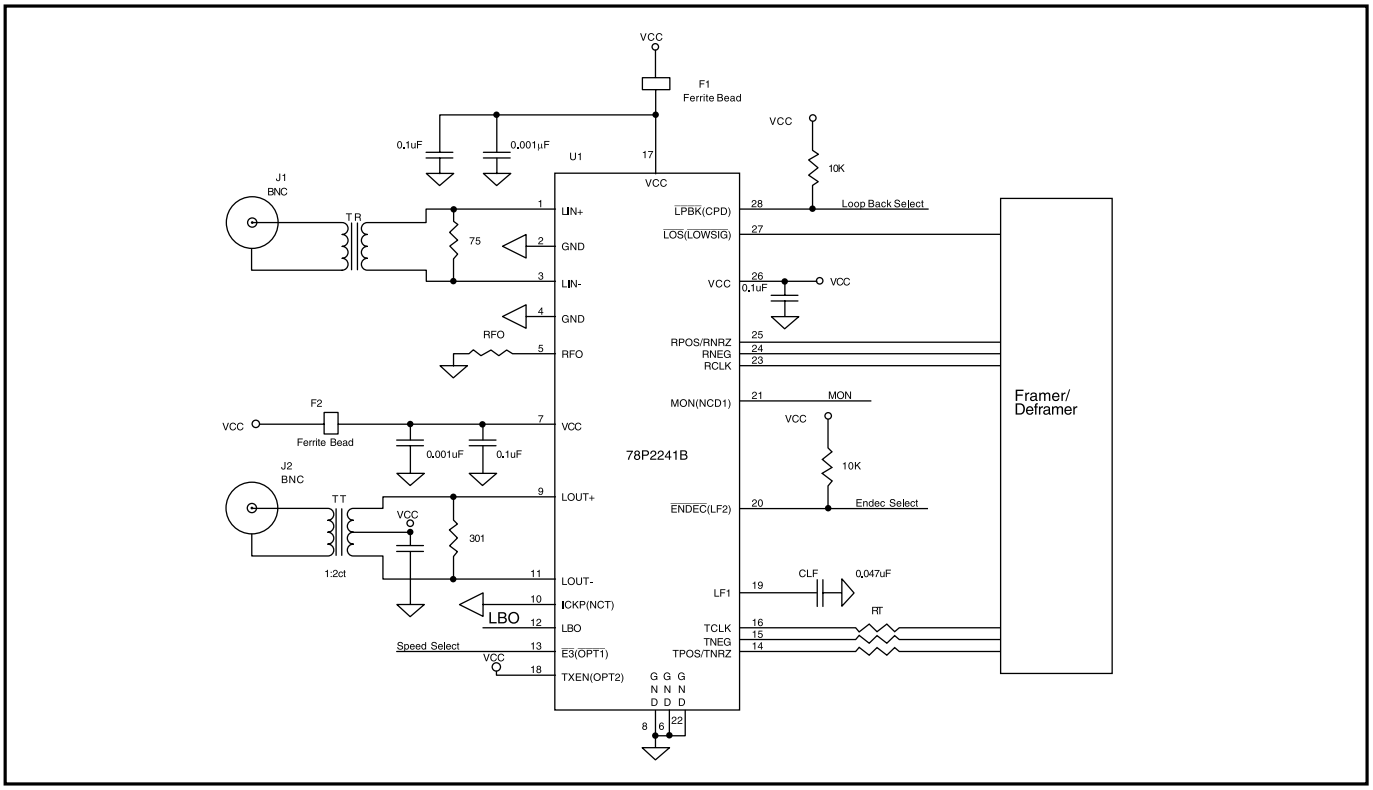
TRANSMITTER OUTPUT JITTER

The transmit jitter specification ensures compliance with ITU-T G.823 and G.824, and ANSI T1.102-199 for all supported rates. Transmit output jitter is not tested during production test.



PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Transmitter Output Jitter	10 Hz to 800 kHz			0.1	UI

E3/DS3/STS-1 Example Circuit



Note 9: Pin names in ( ) denote pin names from 78P7200. Pin numbers refer to 28 PLCC package. Default settings used to simulate 78P7200.

Note 10: Resistors on TCLK, TNEG, TPOS are optional but recommended. Clock pulse shapes at the inputs to the 78P2241B are dependent on board layout and will dictate the need for such added resistors.

Note 11. Adding a series Ferrite Bead on VCC pins may be required for some pc board layout.

EXTERNAL COMPONENTS (Common to E3/DS3/STS-1)

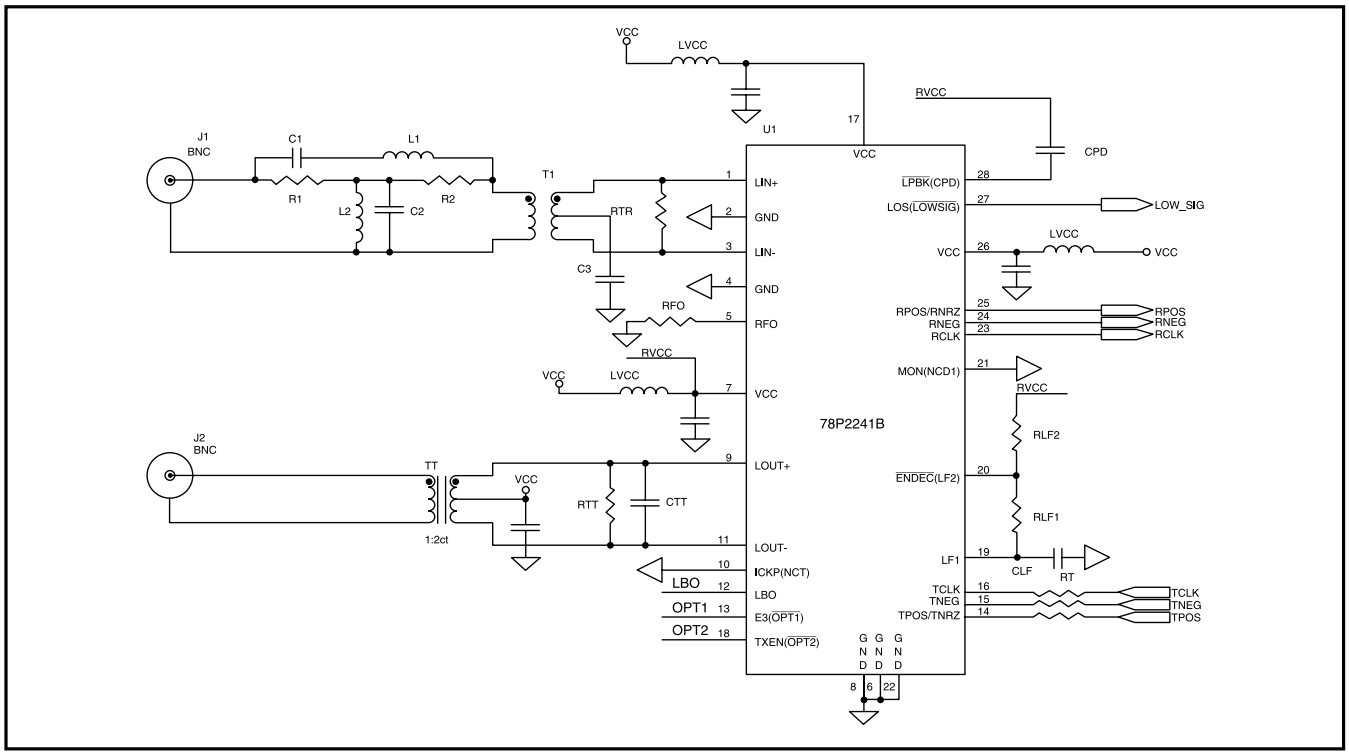
Component		Tolerance	Value	Unit
Receiver Termination Resistor	RTR	1%	75	Ω
Receiver Transformer Turns Ratio	TR	3%	1:1	---
Transmitter Termination Resistor	RTT	1%	301	Ω
Transmitter Transformer Turns Ratio	TT	3%	1:2ct	---

EXTERNAL COMPONENTS (Dependant on speed, nominal value)

Component		Tolerance	STS-1	DS3	E3	Unit
Loop Filter Capacitor	CLF	10%	0.047	0.047	0.047	µF
Bias Resistor	RFO	1%	4.53	5.23	6.81	kΩ

Note 11: Advanced Data sheet pin assignment, functions and external component values are subject to change.

78P2241B Replacement for Existing 78P7200 Designs



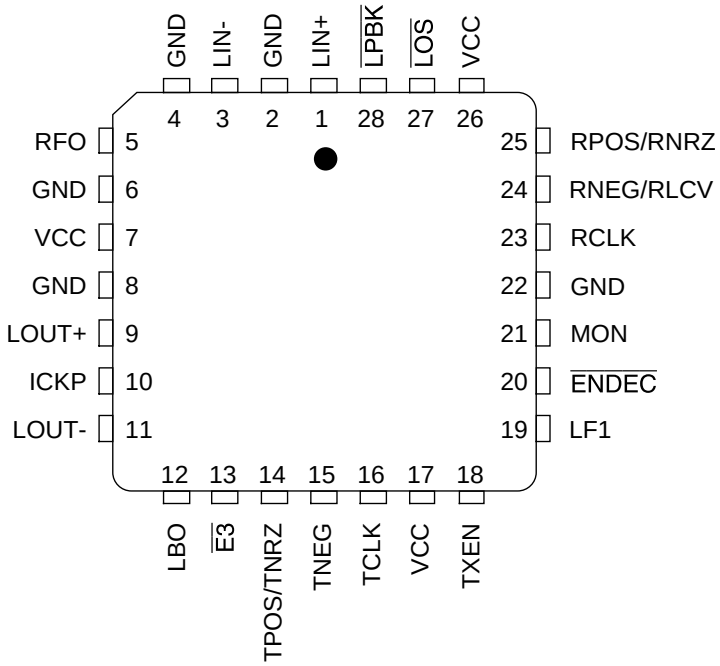
Note 12: 78P7200 components (such as transmitter transformer), which are not shown here, are not modified.

Component Variation for Existing 78P7200 Designs

	COMPONENT	78P7200		78P2241B
INPUT FILTER	R1,R2	75Ω		SHORT (0Ω)
	C2	82p		NOT INSTALLED
	L2	6.8u		NOT INSTALLED
	L1	0.47u		NOT INSTALLED
	C1	1000p		NOT INSTALLED
	C3	0.01		NOT INSTALLED
	T1	1:2		1:1
	RTR	422Ω		75Ω
	CPD	0.22u		SHORT (0Ω)
PLL FILTER	RLF2	100kΩ		NOT INSTALLED
	RLF1	6.04kΩ		NOT INSTALLED
	CLF1	0.22u		0.047u
TRANSMITTER	RTT	DS3	301Ω	301Ω
		E3	604Ω	301Ω
	CTT	DS3	5-15pF	NOT INSTALLED
		E3	3pF	NOT INSTALLED
POWER SUPPLY	LVCC	4.7uH		SHORT (0Ω) or Ferrite Bead

PACKAGE PIN DESIGNATIONS

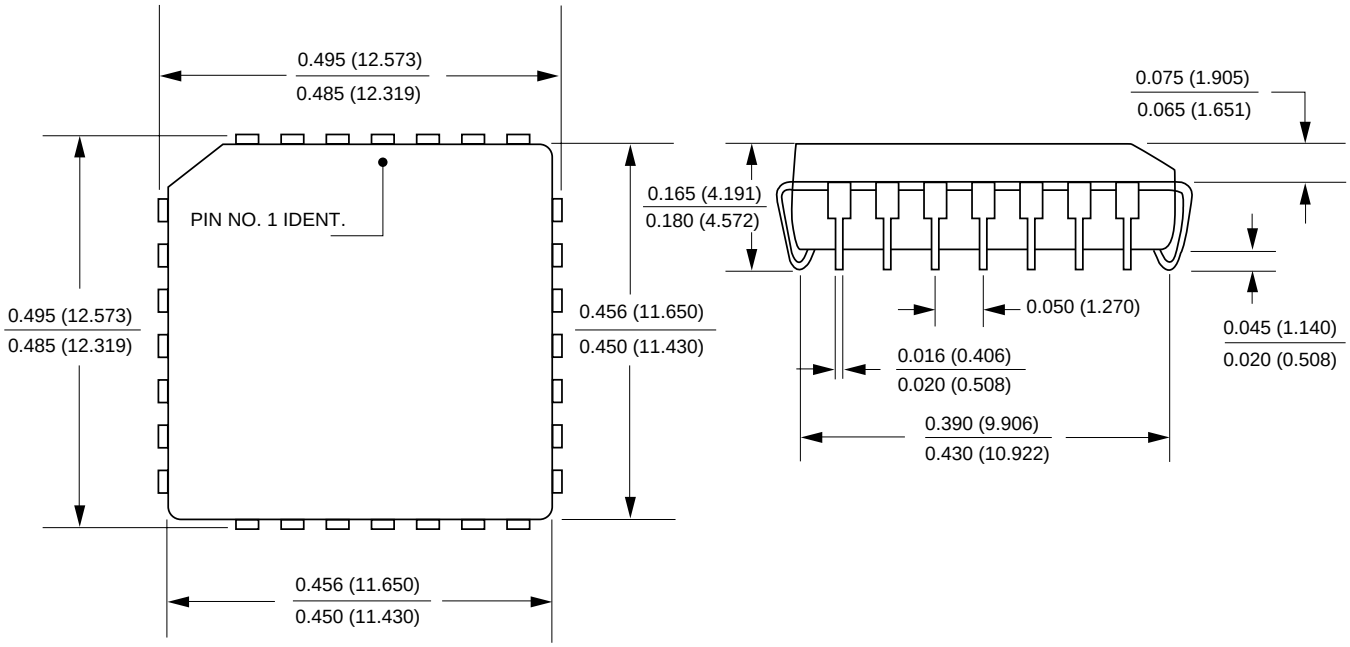
(Top View)



78P2241B
28-Pin PLCC

MECHANICAL DRAWING

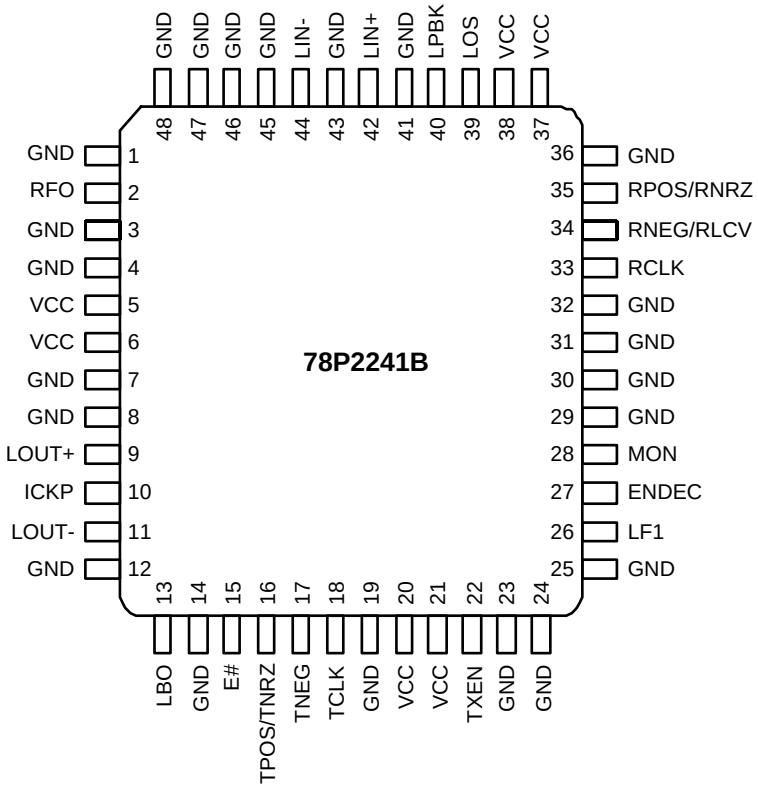
28-Pin PLCC



CAUTION: Use handling procedures necessary for a static sensitive component.

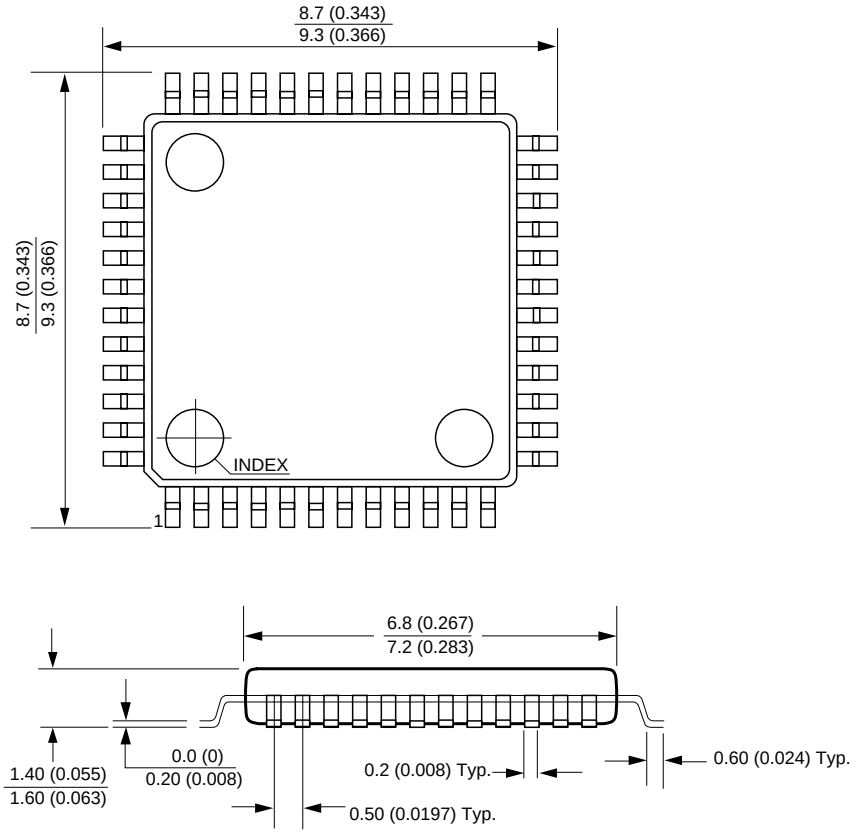
PACKAGE PIN DESIGNATIONS

(Top View)



48-Pin TQFP (JEDEC LQFP)
(NOT pin-compatible to 78P7200)

MECHANICAL DRAWING
48-Pin TQFP (JEDEC LQFP)



ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
28-pin PLCC	78P2241B-IH	78P2241B-IH xxxxxx
28-pin PLCC lead free	78P2241B-IH/F	78P2241B-IH xxxxxxF
48-pin TQFP	78P2241B-IGT	78P2241B-IGT xxxxxx
48-pin TQFP lead free	78P2241B-IGT/F	78P2241B-IGT xxxxxxF

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