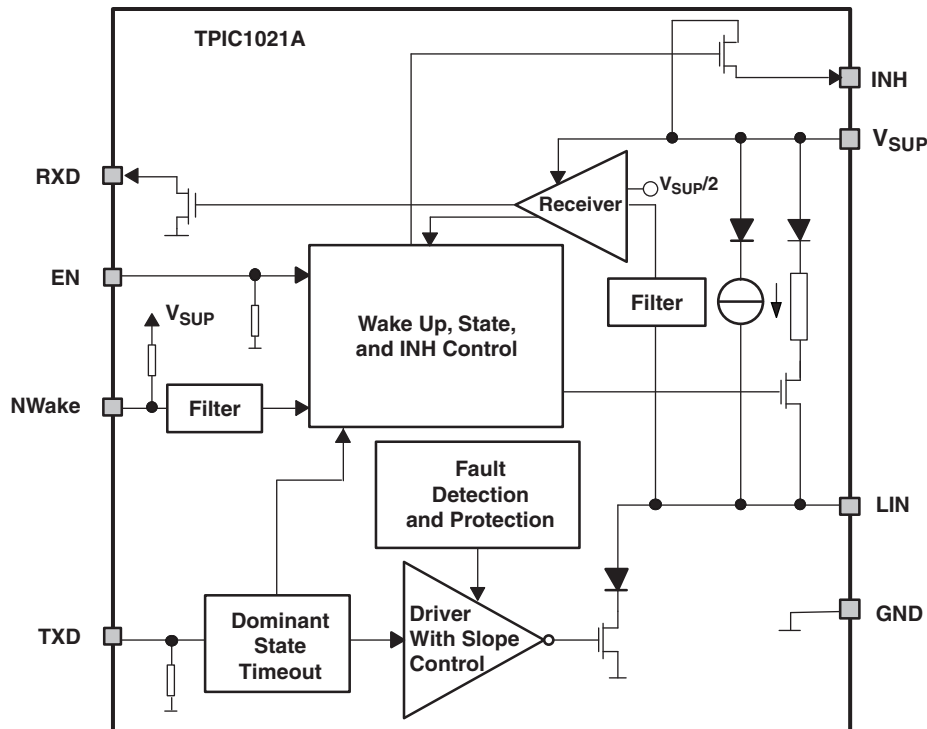


LIN PHYSICAL INTERFACE

FEATURES

- LIN Physical Layer Specification Revision 2.0 Compliant and Conforms to SAEJ2602 Recommended Practice for LIN
- LIN Bus Speed up to 20-kbps LIN Specified Maximum
- Sleep Mode: Ultralow Current Consumption, Allows Wake-Up Events From LIN Bus, Wake-Up Input (External Switch), or Host MCU
- High-Speed Receive Capable
- ESD Protection to ± 12 kV (Human-Body Model) on LIN Pin
- LIN Pin Handles Voltage From -40 V to 40 V
- Survives Transient Damage in Automotive Environment (ISO 7637)
- Extended Operation With Supply From 7 V to 27 V DC (LIN Specification 7 V to 18 V)
- Interfaces to MCU With 5-V or 3.3-V I/O Pins
- Dominant State Timeout Protection
- Wake-Up Request on RXD Pin
- Control of External Voltage Regulator (INH Pin)
- Integrated Pullup Resistor and Series Diode for LIN Slave Applications
- Low Electromagnetic Emission (EME), High Electromagnetic Immunity (EMI)
- Bus Terminal Short Circuit Protected for Short to Battery or Short to Ground
- Thermally Protected
- Ground Disconnection Fail Safe at System Level
- Ground Shift Operation at System Level
- Unpowered Node Does Not Disturb the Network
- Supports ISO9141 (K-Line)-Like Functions

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

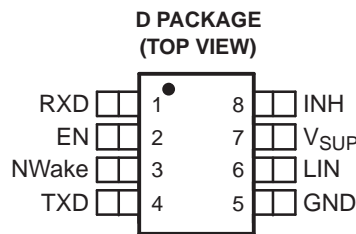
DESCRIPTION

The TPIC1021A is the Local Interconnect Network (LIN) physical interface, which integrates the serial transceiver with wake-up and protection features. The LIN bus is a single-wire bidirectional bus typically used for low-speed in-vehicle networks using data rates between 2.4 kbps and 20 kbps. The LIN protocol output data stream on TXD is converted by the TPIC1021A into the LIN bus signal through a current-limited wave-shaping driver as outlined by the LIN Physical Layer Specification Revision 2.0. The receiver converts the data stream from the LIN bus and outputs the data stream via RXD. The LIN bus has two states: dominant state (voltage near ground) and the recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the TPIC1021A's internal pullup resistor (30 kΩ) and series diode, so no external pullup components are required for slave applications. Master applications require an external pullup resistor (1 kΩ) plus a series diode per the LIN specification.

In sleep mode, the TPIC1021A requires low quiescent current even though the wake-up circuits remain active, allowing for remote wake up via the LIN bus or local wake up via the NWake or EN pins.

The TPIC1021A has been designed for operation in the harsh automotive environment. The device can handle LIN bus voltage swings from 40 V down to ground and survive -40 V. The device also prevents back-feed current through LIN to the supply input, in case of a ground shift or supply voltage disconnection. It also features undervoltage, overtemperature, and loss-of-ground protection. In the event of a fault condition, the output is immediately switched off and remains off until the fault condition is removed.

TERMINAL FUNCTIONS



TERMINAL ASSIGNMENTS

PIN		TYPE	DESCRIPTION
NAME	NO.		
RXD	1	O	RXD output (open drain) interface reporting state of LIN bus voltage
EN	2	I	Enable input
NWake	3	I	High voltage input for device wake up
TXD	4	I	TXD input interface to control state of LIN output
GND	5	GND	Ground
LIN	6	I/O	LIN bus single-wire transmitter and receiver
V _{SUP}	7	Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)
INH	8	O	Inhibit controls external voltage regulator with inhibit input

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
TPIC1021A-Q1	SOIC-8 – D	TPIC1021AQDRQ1 (reel)	T1021A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Local Interconnect Network (LIN) Bus

This I/O pin is the single-wire LIN bus transmitter and receiver.

Transmitter Characteristics

The driver is a low-side transistor with internal current limitation and thermal shutdown. There is an internal 30-k Ω pullup resistor with a serial diode structure to V_{SUP} , so no external pullup components are required for LIN slave mode applications. An external pullup resistor of 1 k Ω , plus a series diode to V_{SUP} must be added when the device is used for master node applications.

Voltage on LIN can go from –40-V to 40-V dc without any currents other than through the pullup resistance. There are no reverse currents from the LIN bus to supply (V_{SUP}), even in the event of a ground shift or loss of supply (V_{SUP}).

The LIN thresholds and ac parameters are LIN Protocol Specification Revision 2.0 compliant.

During a thermal shut down condition the driver is disabled.

Receiver Characteristics

The receiver's characteristic thresholds are ratio-metric with the device supply pin. Typical thresholds are 50%, with a hysteresis between 5% and 17.5% of supply.

The receiver is capable of receiving higher data rates (>100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TPIC1021A to be used for high-speed downloads at end-of-line production or other applications. The actual data rates achievable depend on system time constants (bus capacitance and pullup resistance) and driver characteristics used in the system.

Transmit Input (TXD)

TXD is the interface to the MCU's LIN protocol controller or SCI/UART used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near battery). The TXD input structure is compatible with microcontrollers with 3.3-V and 5-V I/O. TXD has an internal pulldown resistor.

TXD Dominant State Timeout

If TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by TPIC1021A's dominant state timeout timer. This timer is triggered by a falling edge on TXD. If the low signal remains on TXD for longer than t_{DST} , the transmitter is disabled, thus allowing the LIN bus to return to the recessive state and communication to resume on the bus. The timer is reset by a rising edge on TXD.

Receive Output (RXD)

RXD is the interface to the MCU's LIN protocol controller or SCI/UART, which reports the state of the LIN bus voltage. LIN recessive (near battery) is represented by a high level on RXD and LIN dominant (near ground) is represented by a low level on RXD. The RXD output structure is an open-drain output stage. This allows the TPIC1021A to be used with 3.3-V and 5-V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pullup, an external pullup resistor to the microcontroller I/O supply voltage is required.

RXD Wake-up Request

When the TPIC1021A has been in low-power mode and encounters a wake-up event from the LIN bus or NWake pin, RXD goes low, while the device enters and remains in standby mode (until EN is reasserted high and the device enters normal mode).

Supply Voltage (V_{SUP})

V_{SUP} is the TPIC1021A device power supply pin. V_{SUP} is connected to the battery through an external reverse battery blocking diode. The characterized operating voltage range for the TPIC1021A is from 7 V to 27 V. V_{SUP} is protected for harsh automotive conditions up to 40 V.

The device contains a reset circuit to avoid false bus messages during undervoltage conditions when V_{SUP} is less than V_{SUP_UNDER} .

Ground (GND)

GND is the TPIC1021A device ground connection. The TPIC1021A can operate with a ground shift as long as the ground shift does not reduce V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the TPIC1021A does not have a significant current consumption on LIN bus.

Enable Input (EN)

EN controls the operation mode of the TPIC1021A (normal or sleep mode). When EN is high, the TPIC1021A is in normal mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after being woken up. EN has an internal pulldown resistor to ensure the device remains in low-power mode even if EN floats.

NWake Input (NWake)

NWake is a high-voltage input used to wake up the TPIC1021A from low-power mode. NWake is usually connected to an external switch in the application. A low on NWake that is asserted longer than the filter time (t_{NWAKE}) results in a local wake-up. NWake provides an internal pullup source to V_{SUP} .

Inhibit Output (INH)

INH is used to control an external voltage regulator that has an inhibit input. When the TPIC1021A is in normal operating mode, the inhibit high-side switch is enabled and the external voltage regulator is activated. When TPIC1021A is in low-power mode, the inhibit switch is turned off, which disables the voltage regulator. A wake-up event on for the TPIC1021A returns INH to V_{SUP} level. INH can also drive an external transistor connected to an MCU interrupt input.

OPERATING STATES

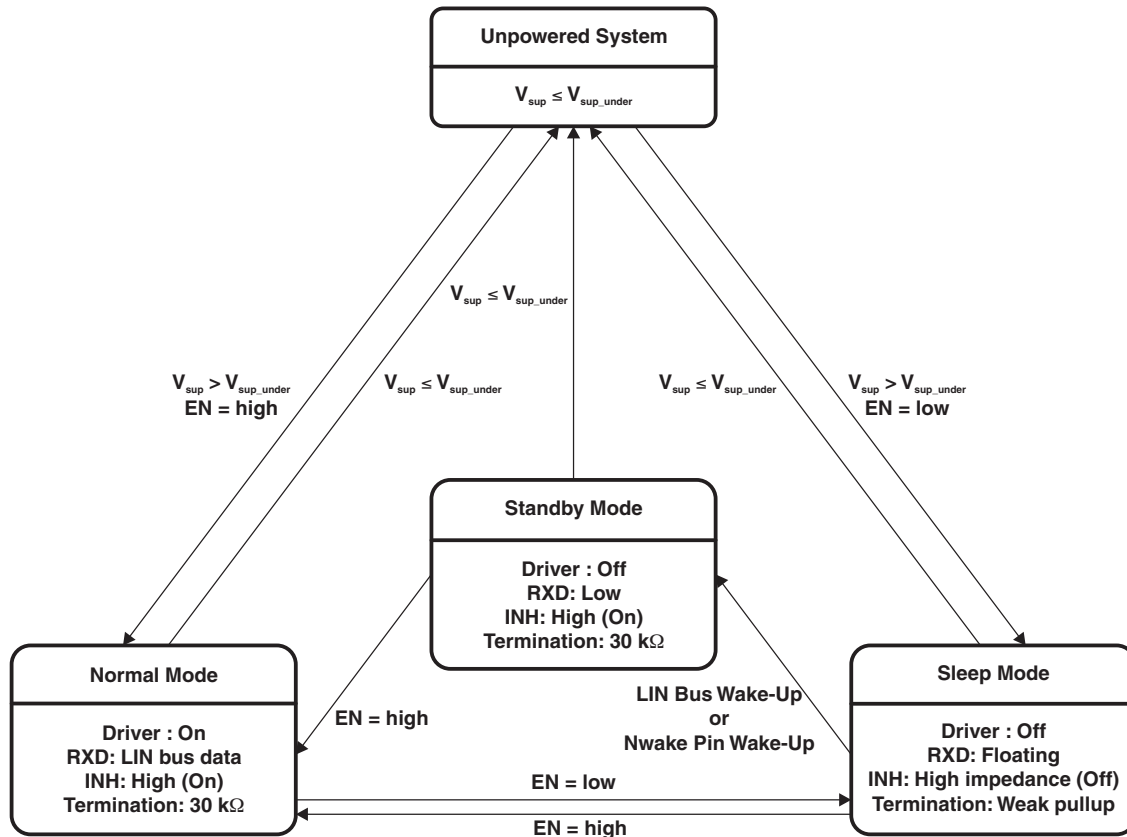


Figure 1. Operating States Diagram

Table 1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	INH	TRANSMITTER	COMMENTS
Sleep	Low	Floating	Weak current pullup	High impedance	Off	
Standby	Low	Low	30 k Ω (typ)	High	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LIN bus data	30 k Ω (typ)	High	On	LIN transmission up to 20 kbps

Normal Mode

This is the normal operational mode, in which the receiver and driver are active, and LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller, where recessive on the LIN bus is a digital high, and dominate on the LIN bus is digital low. The driver transmits input data on TXD to the LIN bus. Normal mode is entered as EN transitions high while the TPIC1021A is in sleep or standby mode.

Sleep Mode

Sleep mode is the power saving mode for the TPIC1021A and the default state after power up (assuming EN is low during power up). Even with the extremely low current consumption in this mode, the TPIC1021A can still wake up from LIN bus via a wake-up signal, a low on NWake, or if EN is set high. The LIN bus and NWake are filtered to prevent false wake-up events. The wake-up events must be active for their respective time periods (t_{LINBUS} , t_{NWake}).

The sleep mode is entered by setting EN low.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pullup is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- INH is high impedance.
- EN input, NWake input, and the LIN wake-up receiver are active.

Wake-Up Events

There are three ways to wake up the TPIC1021A from sleep mode:

- Remote wake-up via recessive (high) to dominant (low) state transition on LIN bus. The dominant state must be held for t_{LINBUS} filter time and then the bus must return to the recessive state (to eliminate false wake-ups from disturbances on the LIN bus or if the bus is shorted to ground).
- Local wake-up via a low on NWake, which is asserted low longer than the filter time t_{NWake} (to eliminate false wake-ups from disturbances on NWake)
- Local wake-up via EN being set high

Standby Mode

This mode is entered whenever a wake-up event occurs via LIN bus or NWake while the TPIC1021A is in sleep mode. The LIN bus slave termination circuit and INH are turned on when standby mode is entered. The application system powers up once INH is turned on, assuming the system is using a voltage regulator connected via INH. Standby mode is signaled via a low level on RXD.

When EN is set high while the TPIC1021A is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

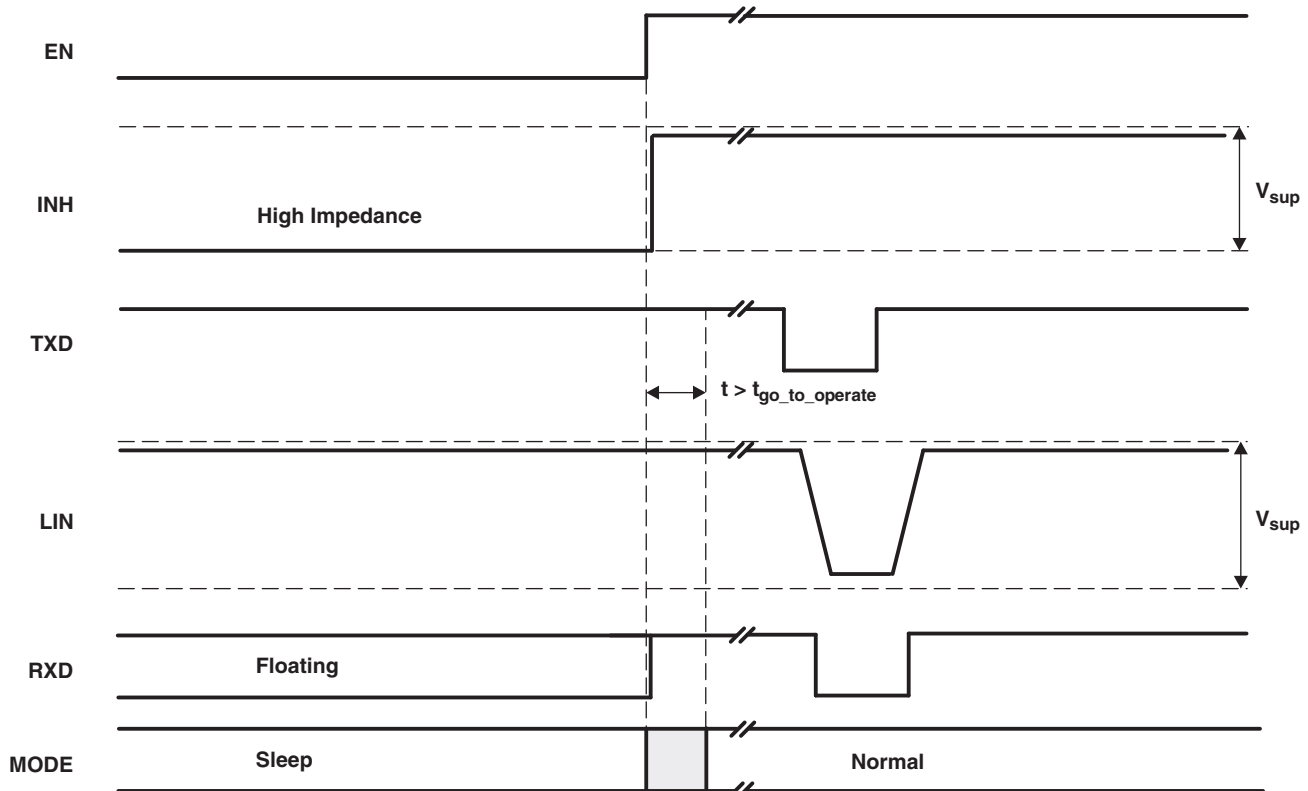


Figure 2. Wake-Up Via EN

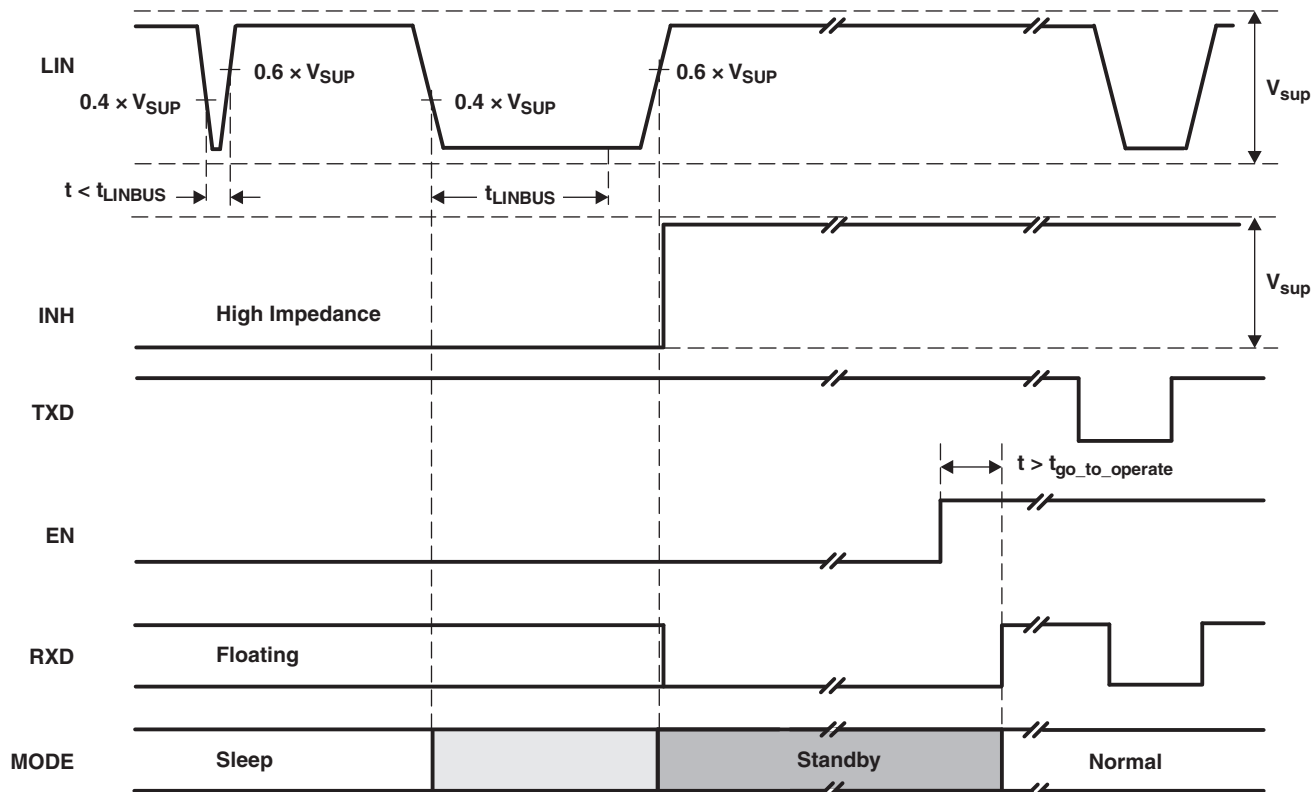


Figure 3. Wake-Up Via LIN

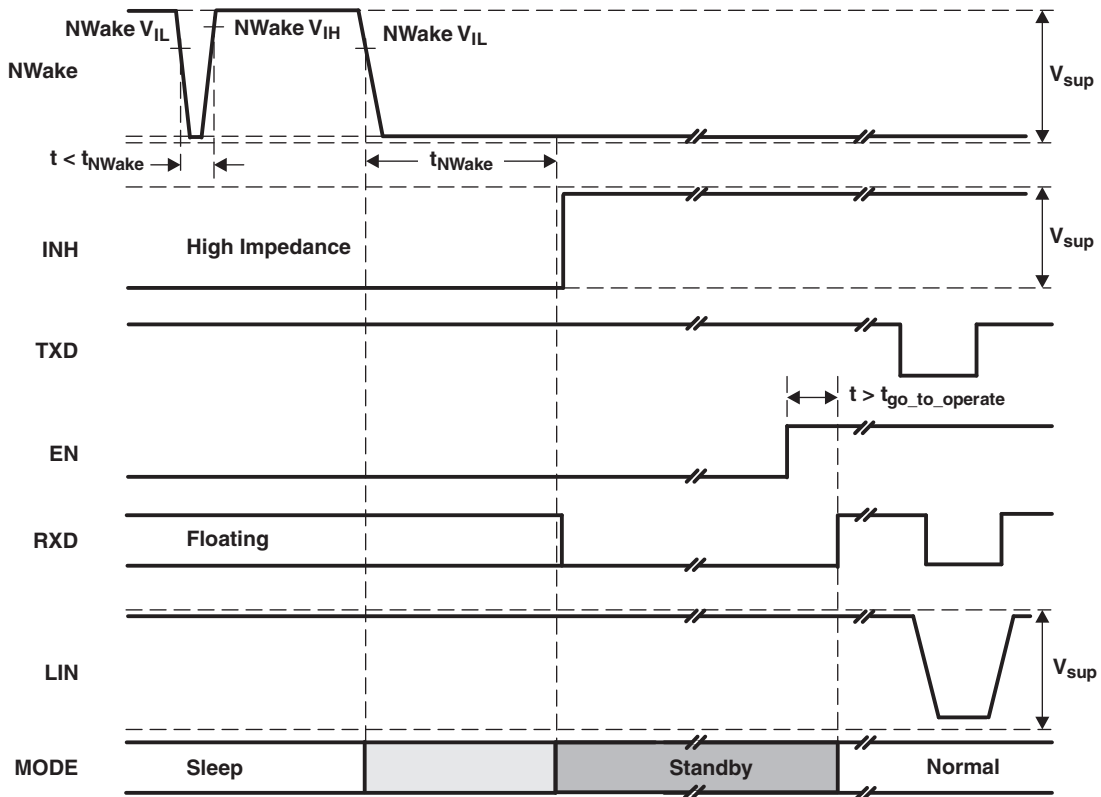


Figure 4. Wake-Up Via NWake

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER		RATING	UNIT	
$V_{SUP}^{(2)}$	Supply line supply voltage ⁽³⁾	0 to 40	V	
V_{NWake}	NWake dc and transient input voltage (through 33-k Ω serial resistor)	–0.3 to 40		
I_{NWake}	NWake current if due to ground shifts $V_{NWake} \leq V_{GND} - 0.3V$, thus the current into NWake must –3.6 mA be limited via a serial resistance.	–3.6	mA	
V_{INH}	INH voltage	–0.3 to $V_{SUP} + 0.3$	V	
	Logic pin input voltage RXD, TXD, EN	–0.3 to 5.5		
V_{LIN}	LIN dc-input voltage	–40 to 40	kV	
Electrostatic discharge	Human-Body Model	LIN ⁽⁴⁾		–12 to 12
		NWake ⁽⁴⁾		–11 to 11
	Charge-Device Model	All other pins ⁽⁴⁾		–4 to 4
		All pins ⁽⁵⁾	–1500 to 1500	V
T_A	Operational free-air temperature range	–40 to 125	°C	
T_J	Junction temperature range	–40 to 150		
T_{stg}	Storage temperature range	–40 to 165		
$R_{\theta JA}$	Thermal resistance, junction to ambient	145	°C/W	
	Thermal shutdown	200	°C	
	Thermal shutdown hysteresis	25		

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) The device is specified for operation in the range of V_{SUP} from 7 V to 27 V. Operating the device above 27 V may significantly raise the junction temperature of the device and system level thermal design needs to be considered.
- (4) The human body model is a 100-pF capacitor discharged through a 1.5-k Ω resistor into each pin.
- (5) Tested in accordance to JEDEC Standard 22, Test Method C101 (JESD22-C101).

ELECTRICAL CHARACTERISTICS

V_{SUP} = 7 V to 27 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
SUPPLY						
	Operational supply voltage ⁽²⁾	Device is operational beyond the LIN 2.0 defined nominal supply line voltage range of 7 V < V _{SUP} < 18 V	7	14	27	V
	Nominal supply line voltage	Normal and standby modes	7	14	18	
		Sleep mode	7	12	18	
	V _{SUP} undervoltage threshold			4.5	6.2	
I _{CC}	Supply current	Normal mode, EN = High, Bus dominant (total bus load where R _{LIN} ≥ 500 Ω and C _{LIN} ≤ 10 nF (see Figure 7) ⁽³⁾ , INH = V _{SUP} , NWake = V _{SUP}		1.2	7.5	mA
		Standby mode, EN = Low, Bus dominant (total bus load, where R _{LIN} ≥ 500 Ω and C _{LIN} ≤ 10 nF (see Figure 7) ⁽³⁾ , INH = V _{SUP} , NWake = V _{SUP}		1	2.1	mA
		Normal mode, EN = High, Bus recessive, LIN = V _{SUP} , INH = V _{SUP} , NWake = V _{SUP}		450	775	μA
		Standby mode, EN = Low, Bus recessive, LIN = V _{SUP} , INH = V _{SUP} , NWake = V _{SUP}		450	775	
		Sleep mode, EN = 0, 7 V < V _{SUP} ≤ 12 V, LIN = V _{SUP} , NWake = V _{SUP}		15	30	μA
		Sleep mode, EN = 0, 12 V < V _{SUP} < 27 V, LIN = V _{SUP} , NWake = V _{SUP}			50	μA
RXD OUTPUT PIN						
V _O	Output voltage		–0.3		5.5	V
I _{OL}	Low-level output current, open drain	LIN = 0 V, RXD = 0.4 V	3.5			mA
I _{IKG}	Leakage current, high-level	LIN = V _{SUP} , RXD = 5 V	–5	0	5	μA
TXD INPUT PIN						
V _{IL}	Low-level input voltage		–0.3		0.8	V
V _{IH}	High-level input voltage		2		5.5	
V _{IT}	Input threshold hysteresis voltage		30		500	mV
	Pulldown resistor		125	350	800	kΩ
I _{IL}	Low-level input current	TXD = Low	–5	0	5	μA

- (1) Typical values are given for V_{SUP} = 14 V at 25°C, except for low power mode where typical values are given for V_{SUP} = 12 V at 25°C.
- (2) All voltages are defined with respect to ground; positive currents flow into the TPIC1021A device.
- (3) In the dominant state, the supply current increases as the supply voltage increases due to the integrated LIN slave termination resistance. At higher voltages the majority of supply current is through the termination resistance. The minimum resistance of the LIN slave termination is 20 kΩ, so the maximum supply current attributed to the termination is:

$$I_{SUP (dom) \text{ max termination}} \approx (V_{SUP} - (V_{LIN_Dominant} + 0.7 \text{ V}) / 20 \text{ k}\Omega$$

ELECTRICAL CHARACTERISTICS (continued)
 $V_{SUP} = 7\text{ V to }27\text{ V}$, $T_A = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
LIN PIN (Referenced to V_{SUP})						
V_{OH}	High-level output voltage	LIN recessive, TXD = High, $I_O = 0\text{ mA}$, $V_{SUP} = 14\text{ V}$	$V_{SUP} - 1$			V
V_{OL}	Low-level output voltage	LIN dominant, TXD = Low, $I_O = 40\text{ mA}$, $V_{SUP} = 14\text{ V}$	0		$0.2 \times V_{SUP}$	V
R_{slave}	Pullup resistor to V_{SUP}	Normal and standby modes	20	30	60	k Ω
	Pullup current source to V_{SUP}	Sleep mode, $V_{SUP} = 14\text{ V}$, LIN = GND	-2		-20	μA
I_L	Limiting current	TXD = 0 V	45	160	250	mA
I_{LKG}	Leakage current	LIN = V_{SUP}	-5	0	5	μA
I_{LKG}	Leakage current, loss of supply	7 V < LIN \leq 12 V, $V_{SUP} = \text{GND}$ 12 V < LIN < 18 V, $V_{SUP} = \text{GND}$			5 10	
V_{IL}	Low-level input voltage	LIN dominant			$0.4 \times V_{SUP}$	V
V_{IH}	High-level input voltage	LIN recessive	$0.6 \times V_{SUP}$			
V_{IT}	Input threshold voltage		$0.4 \times V_{SUP}$	$0.5 \times V_{SUP}$	$0.6 \times V_{SUP}$	
V_{hys}	Hysteresis voltage		$0.05 \times V_{SUP}$		$0.175 \times V_{SUP}$	
V_{IL}	Low-level input voltage for wake-up				$0.4 \times V_{SUP}$	
EN PIN						
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{IH}	High-level input voltage		2		5.5	
V_{hys}	Hysteresis voltage		30		500	mV
	Pulldown resistor		125	350	800	k Ω
I_{IL}	Low-level input current	EN = Low	-5	0	5	μA
INH PIN						
V_o	DC output voltage		-0.3		$V_{SUP} + 0.3$	V
R_{on}	On state resistance	Between V_{SUP} and INH, INH = 2-mA drive, Normal or standby mode		35	85	Ω
I_{IKG}	Leakage current	Low-power mode, $0 < \text{INH} < V_{SUP}$	-5	0	5	μA
NWake PIN						
V_{IL}	Low-level input voltage		-0.3		$V_{SUP} - 3.3$	V
V_{IH}	High-level input voltage		$V_{SUP} - 1$		$V_{SUP} + 0.3$	
	Pullup current	NWake = 0 V	-45	-10	-2	μA
I_{IKG}	Leakage current	$V_{SUP} = \text{NWake}$	-5	0	5	
THERMAL SHUTDOWN						
	Shutdown junction thermal temperature			190		$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (continued)

V_{SUP} = 7 V to 27 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
AC CHARACTERISTICS						
D1	Duty cycle 1 ⁽⁴⁾	TH _{REC(max)} = 0.744 × V _{SUP} , TH _{DOM(max)} = 0.581 × V _{SUP} , V _{SUP} = 7 V to 18 V, t _{BIT} = 50 μs (20 kbps), D1 = t _{Bus_rec(min)} / (2 × t _{BIT}). See Figure 5	0.396			
D2	Duty cycle 2 ⁽⁴⁾	TH _{REC(min)} = 0.422 × V _{SUP} , TH _{DOM(min)} = 0.284 × V _{SUP} , V _{SUP} = 7.6 V to 18 V, t _{BIT} = 50 μs (20 kbps), D2 = t _{Bus_rec(max)} / (2 × t _{BIT}). See Figure 5			0.581	
D3	Duty cycle 3 ⁽⁴⁾	TH _{REC(max)} = 0.778 × V _{SUP} , TH _{DOM(max)} = 0.616 × V _{SUP} , V _{SUP} = 7 V to 18 V, t _{BIT} = 96 μs (10.4 kbps), D3 = t _{Bus_rec(min)} / (2 × t _{BIT}). See Figure 5	0.417			
D4	Duty cycle 4 ⁽⁴⁾	TH _{REC(min)} = 0.389 × V _{SUP} , TH _{DOM(min)} = 0.251 × V _{SUP} , V _{SUP} = 7.6 V to 18 V, t _{BIT} = 96 μs (10.4 kbps), D4 = t _{Bus_rec(max)} / (2 × t _{BIT}). See Figure 5			0.59	
t _{rx_pdr}	Receiver rising propagation delay time	R _{RXD} = 2.4 kΩ, C _{RXD} = 20 pF See Figure 6 See Figure 7			6	μs
t _{rx_pdf}	Receiver falling propagation delay time	R _{RXD} = 2.4 kΩ, C _{RXD} = 20 pF See Figure 6 See Figure 7			6	
t _{rx_sym}	Symmetry of receiver propagation delay time	rising edge with respect to falling edge (t _{rx_sym} = t _{rx_pdf} - t _{rx_pdr}) R _{RXD} = 2.4 kΩ, C _{RXD} = 20 pF See Figure 6 See Figure 7	–2		2	
t _{NWake}	NWake filter time for local wake-up	See Figure 4	25	50	150	
t _{LINBUS}	LIN wake-up filter time (dominant time for wake-up via LIN bus)	See Figure 3	25	50	150	
t _{DST}	Dominant state timeout ⁽⁵⁾		5.5		20	ms
t _{go_to_operate}		See Figure 2 to Figure 3		0.5	1	μs

(4) Duty cycles: LIN driver bus load conditions (C_{LINBUS}, R_{LINBUS}): Load1 = 1 nF, 1 kΩ; Load2 = 10 nF, 500 Ω. Duty cycles 3 and 4 are defined for 10.4-kbps operation. The TPIC1021A also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by Duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification.

(5) Dominant state timeout limits the minimum data rate to 2.4 kbps.

TIMING DIAGRAMS

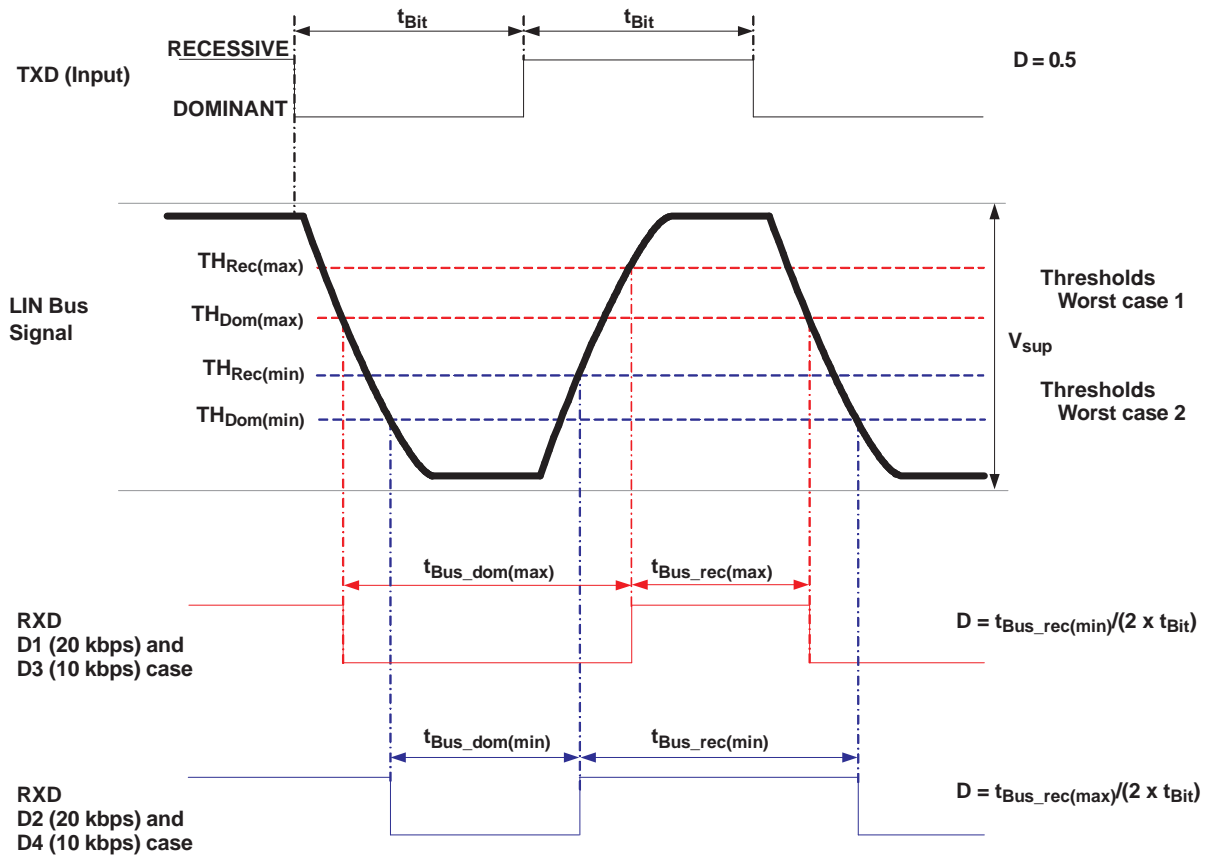


Figure 5. Definition of Bus Timing Parameters

TIMING DIAGRAMS (continued)

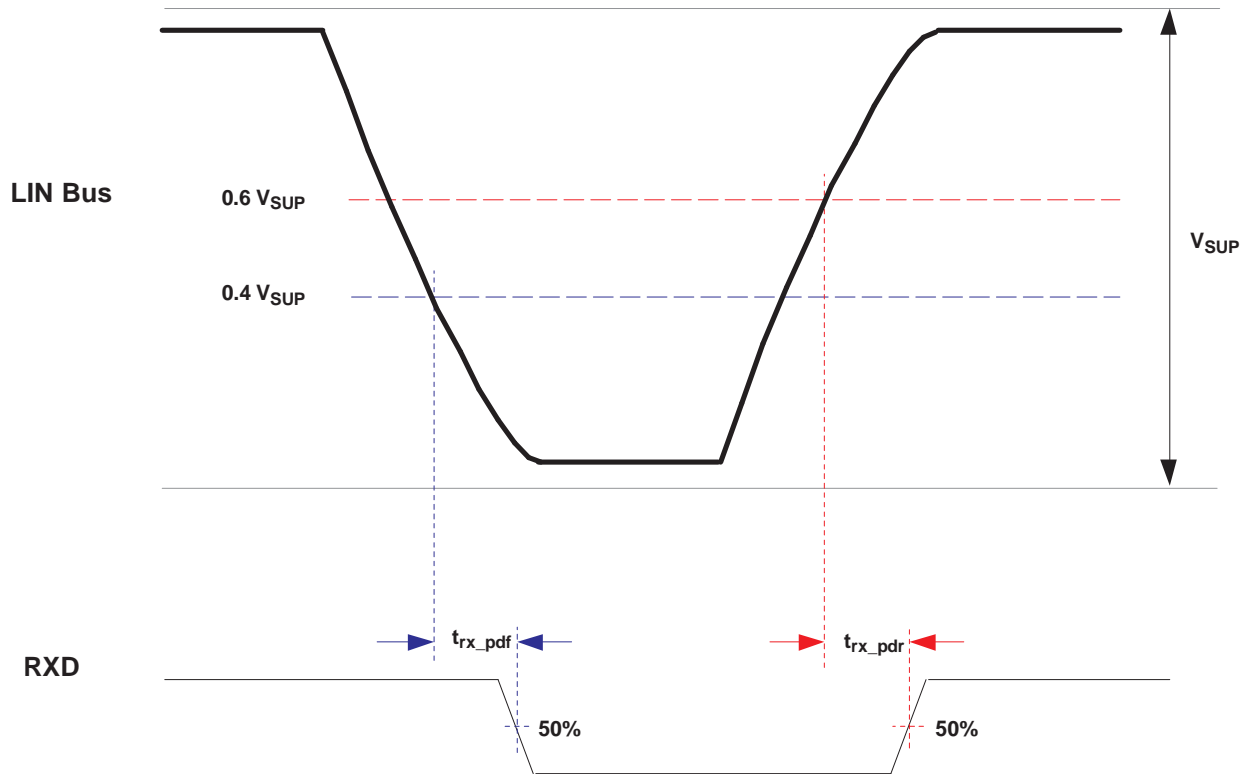


Figure 6. Propagation Delay

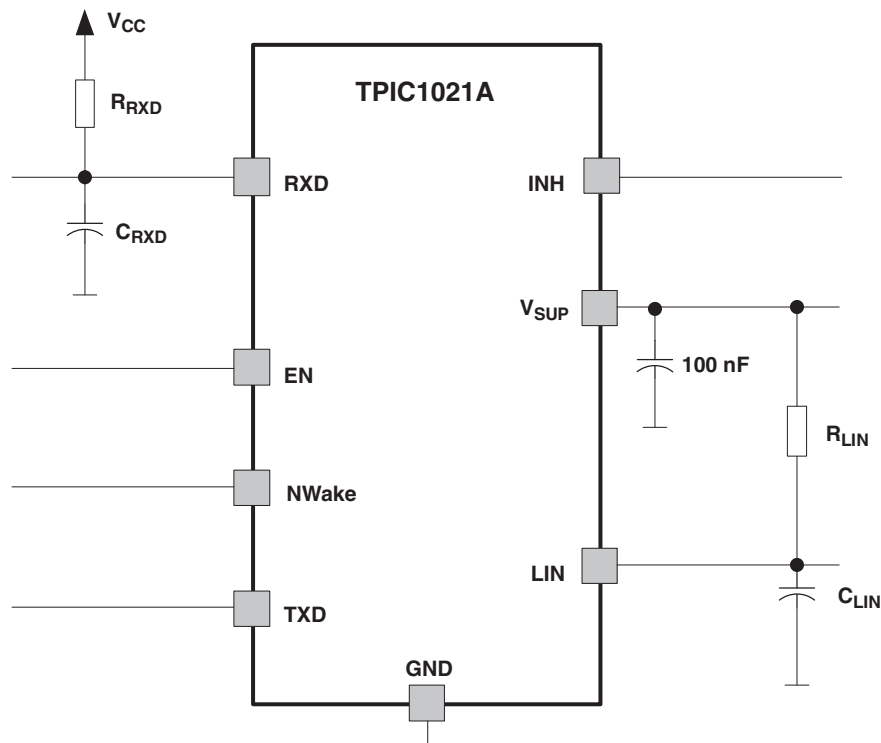
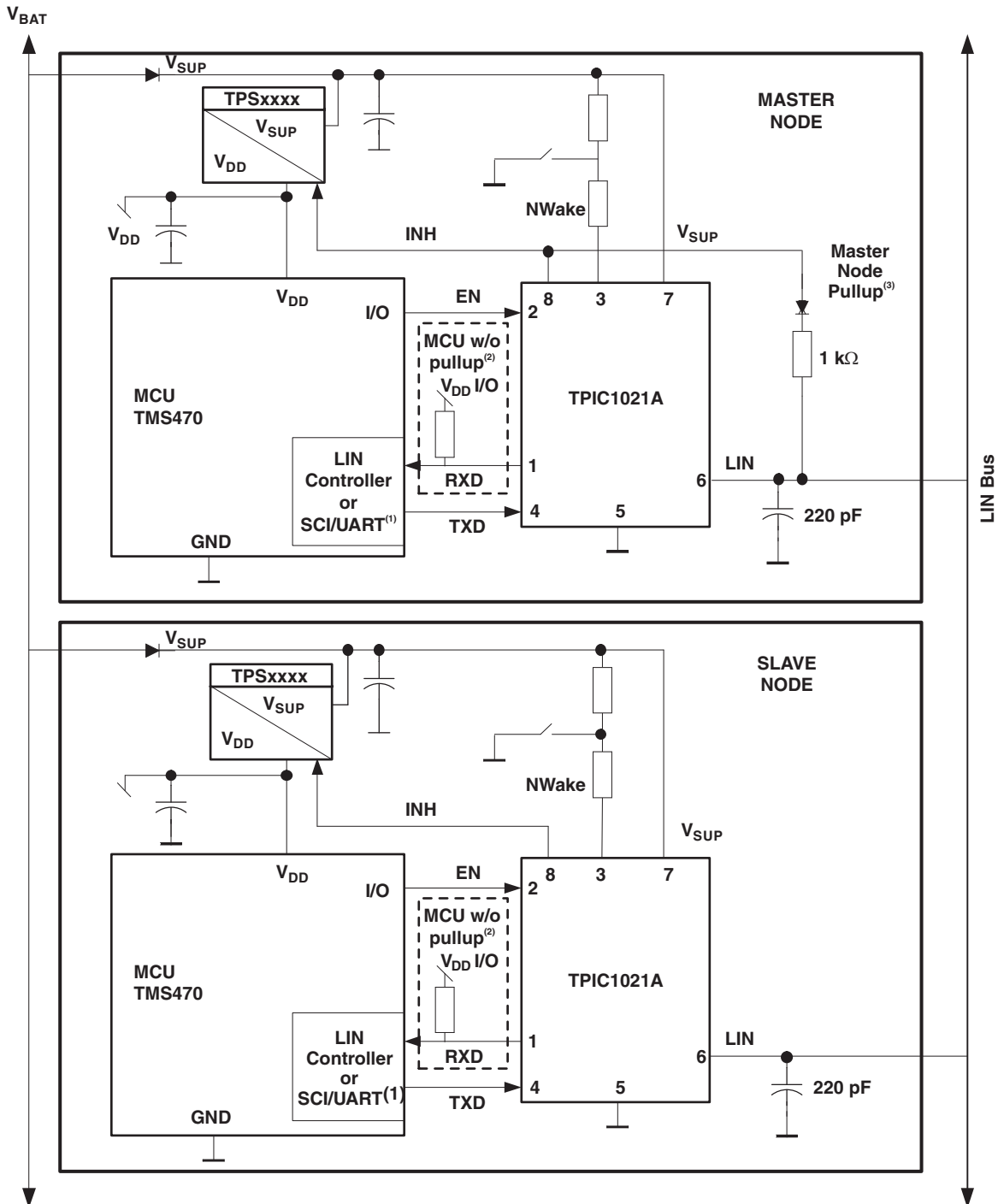


Figure 7. Test Circuit for AC Characteristics

APPLICATION INFORMATION



- (1) RXD on MCU or LIN slave has internal pullup, no external pullup resistor is needed.
- (2) RXD on MCU or LIN slave without internal pullup, requires external pullup resistor.
- (3) Master node applications require an external 1-kΩ pullup resistor and serial diode.

Figure 8.

Device Comparison: TPIC1021 vs TPIC1021A

The TPIC1021A is pin-to-pin compatible to the TPIC1021 device. The TPIC1021A is an enhanced LIN transceiver, including enhanced immunity to RF disturbances. [Table 2](#) is a summary of the differences between the two devices.

Table 2. TPIC1021A vs TPIC1021 Differences

SPECIFICATION	TPIC1021A	TPIC1021
LIN termination	Weak current pullup in sleep mode	High Ω in low-power mode
LIN receiver	Enhanced high-speed receive capable	High-speed receive capable
LIN leakage current (unpowered device): $7\text{ V} < \text{LIN} < 12\text{ V}$, $V_{\text{SUP}} = \text{GND}$	$<5\ \mu\text{A}$ at 12 V (max)	$<10\ \mu\text{A}$ at 12 V (typ)
LIN bus wake-up	Remote wake-up via recessive-to-dominant transition on LIN bus where dominant bus state is held for at least t_{LINBUS} time followed by a transition back to the recessive state	Remote wake-up via recessive-to-dominant transition on LIN bus where dominant bus state is held for at least t_{LINBUS} time
Low-power current	$<30\ \mu\text{A}$ at 12 V (max)	$<50\ \mu\text{A}$ at 14 V (max)
INH pin	Enhanced driving of bus master termination via lower R_{on}	Driving of bus master termination

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPIC1021AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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