

CMOS Analog Switches

FEATURES

- $\pm 15\text{-V}$ Input Range
- Fast Switching— t_{ON} : 110 ns
- Low $r_{DS(on)}$: $30\ \Omega$
- Single Supply Operation
- CMOS Logic Levels
- Micropower: 30 nW

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

DESCRIPTION

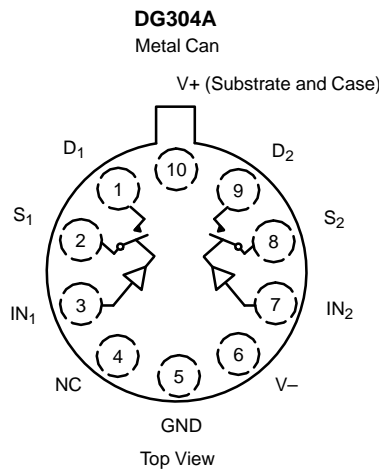
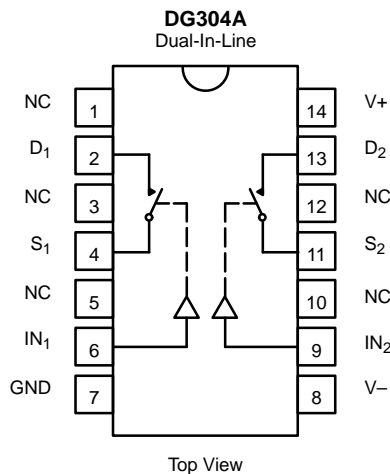
The DG304A through DG307A series of monolithic CMOS switches were designed for applications in communications, instrumentation and process control. This series is well suited for applications requiring fast switching and nearly flat on-resistance over the entire analog range.

applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation (for positive switch voltages) is allowed by connecting the V^- rail to 0 V.

Designed on the Vishay Siliconix PLUS-40 CMOS process to achieve low power consumption and excellent on/off switch performance, these switches are ideal for battery powered

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS input compatible.

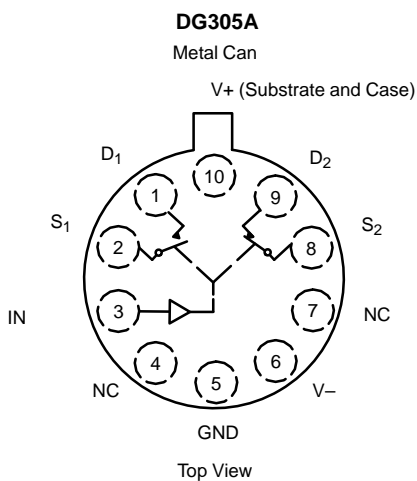
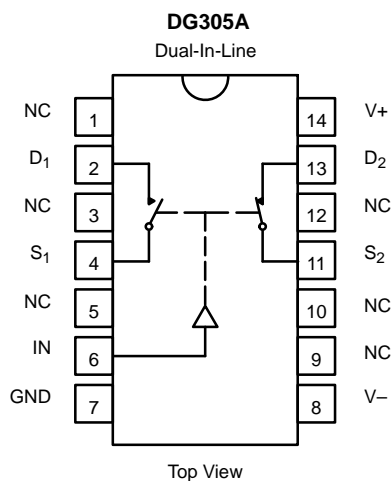
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

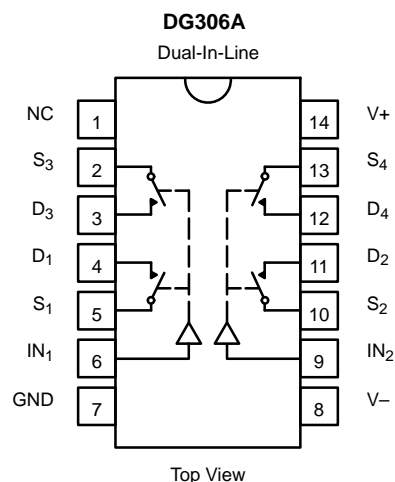
Logic "0" $\leq 3.5\text{ V}$
Logic "1" $\geq 11\text{ V}$

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



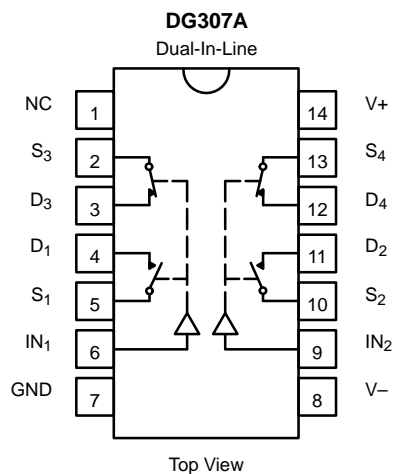
| TRUTH TABLE | | |
|-------------|-----------------|-----------------|
| Logic | SW ₁ | SW ₂ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V



| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V



Four SPST Switches per Package

| TRUTH TABLE | | |
|-------------|-----------------------------------|-----------------------------------|
| Logic | SW ₁ , SW ₂ | SW ₃ , SW ₄ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V



| ORDERING INFORMATION | | |
|----------------------|--------------------|------------------|
| Temp Range | Package | Part Number |
| DG304A | | |
| -0 to 70°C | 14-Pin Plastic DIP | DG304ACJ |
| -55 to 125°C | 14-Pin CerDIP | DG304AAK/883 |
| | | JM38510/11605BCA |
| | 10-Pin Can | JM38510/11605BIA |
| | 14-Pin Sidebrazed | JM38510/11605BCC |
| DG305A | | |
| -55 to 125°C | 14-Pin CerDIP | JM38510/11605BCA |
| | 10-Pin Can | JM38510/11606BIC |
| | 14-Pin Sidebrazed | JM38510/11606BCA |
| DG306A | | |
| -0 to 70°C | 14-Pin Plastic DIP | DG306ACJ |
| -55 to 125°C | 14-Pin CerDIP | DG306AAK/883 |
| | | JM38510/11607BCA |
| | 14-Pin Sidebrazed | JM38510/11607BCC |
| DG307A | | |
| 0 to 70°C | 14-Pin Plastic DIP | DG307ACJ |
| -25 to 85°C | 14-Pin CerDIP | DG307ABK |
| -55 to 125°C | | DG307AAK |
| | | DG307AAK/883 |
| | | JM38510/11608BCA |
| | | JM38510/11608BCC |
| 14-Pin Sidebrazed | JM38510/11608BCC | |

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

Digital Inputs^a, V_S, V_D (V-) -2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal 30 mA

Continuous Current, S or D (Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature (AAA, AAK, ABK Suffix) -65 to 150°C (ACJ Suffix) -65 to 125°C

Power Dissipation^b

14-Pin Plastic DIP^c 470 mW

14-Pin CerDIP^d 825 mW

10-Pin Metal Can^e 450 mW

- Notes:
- a. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - b. All leads welded or soldered to PC Board.
 - c. Derate 11 mW/°C above 75°C
 - d. Derate 6.5 mW/°C above 25°C
 - e. Derate 6 mW/°C above 75°C



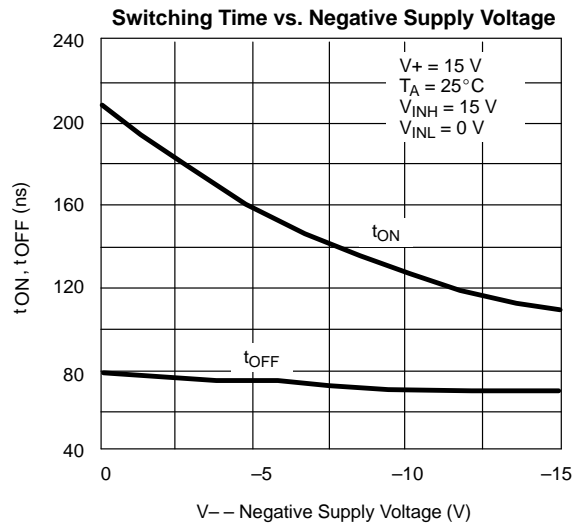
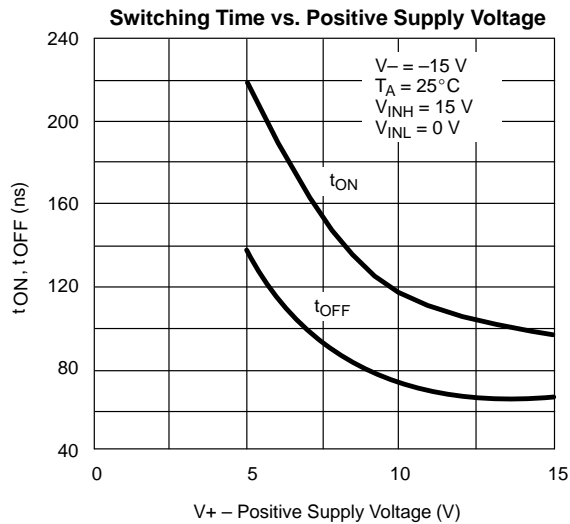
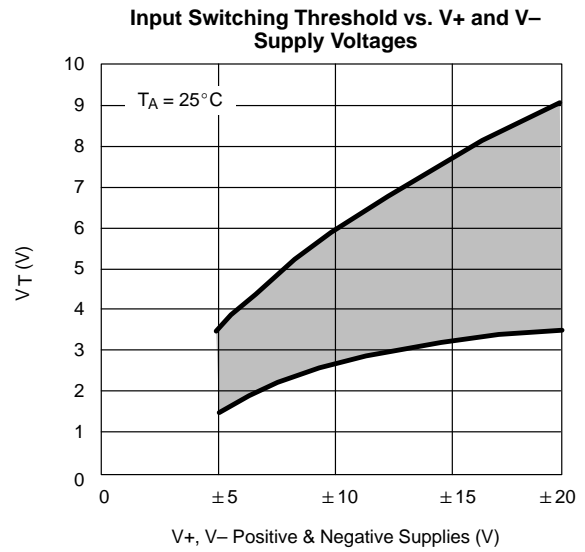
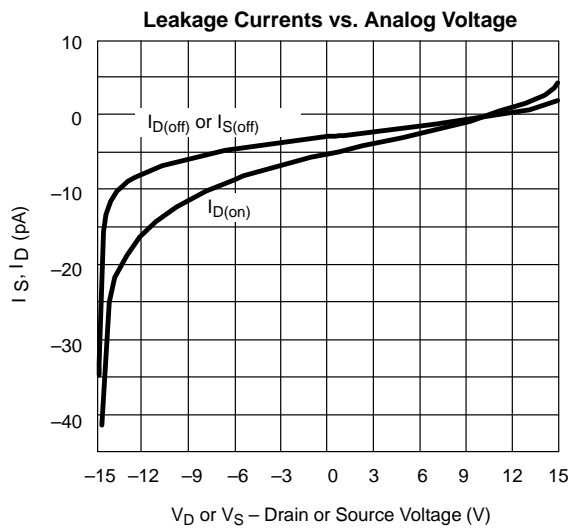
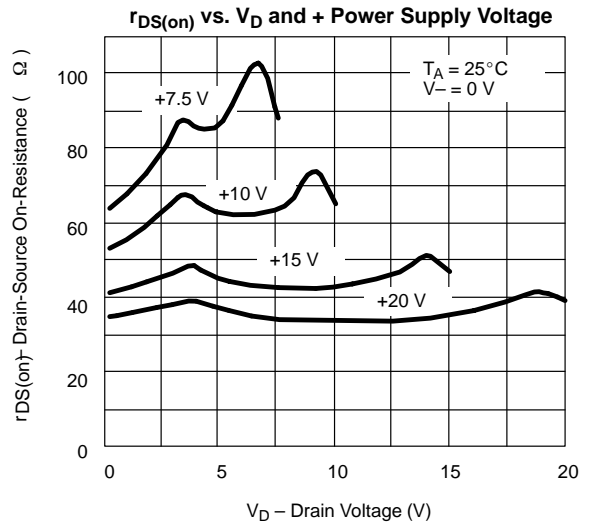
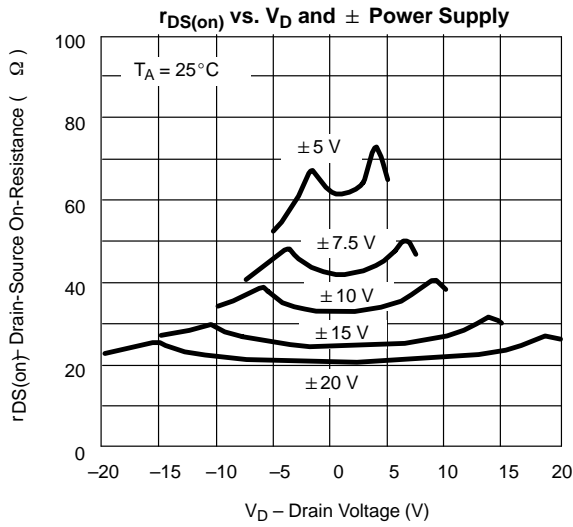
| SPECIFICATIONS ^a | | | | | | | | | |
|---------------------------------------|--------------|---|--------------------|-----------------------|--------------------------|------------------|---|------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_{IN} = 3.5\text{ V}$ or 11 V ^f | Temp ^b | Typ ^c | A Suffix -55 to 125°C | | B, C Suffix -25 to 85°C 0 to 70°C | | Unit |
| | | | | | Min ^d | Max ^d | Min ^d | Max ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | -15 | 15 | -15 | 15 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $V_D = \pm 10\text{ V}$, $I_S = 10\text{ mA}$ | Room Full | 30 | | 50 75 | | 50 75 | Ω |
| Source Off Leakage Current | $I_{S(off)}$ | $V_S = \pm 14\text{ V}$ $V_D = \mp 14\text{ V}$ | Room Full | ± 0.1 | -1 -100 | 1 100 | -5 -100 | 5 100 | nA |
| Drain Off Leakage Current | $I_{D(off)}$ | $V_S = \pm 14\text{ V}$ $V_D = \mp 14\text{ V}$ | Room Full | ± 0.1 | -1 -100 | 1 100 | -5 -100 | 5 100 | |
| Drain On Leakage Current | $I_{D(on)}$ | $V_D = V_S = \pm 14\text{ V}$ | Room Full | ± 0.1 | -2 -200 | 2 200 | -5 -200 | 5 200 | |
| Digital Control | | | | | | | | | |
| Input Current with Input Voltage High | I_{INH} | $V_{IN} = 5\text{ V}$ | Room Full | -0.001 | -1 -1 | | -1 | | μA |
| | | $V_{IN} = 15\text{ V}$ | Room Full | 0.001 | | 1 1 | | 1 | |
| Input Current with Input Voltage Low | I_{INL} | $V_{IN} = 0\text{ V}$ | Room Full | -0.001 | -1 -1 | | -1 | | |
| Dynamic Characteristics | | | | | | | | | |
| Turn-On Time | t_{ON} | See Figure 2 | Room | 110 | | 250 | | | ns |
| Turn-Off Time | t_{OFF} | | Room | 70 | | 150 | | | |
| Break-Before-Make Time | t_{OPEN} | DG305A/307A ONLY See Figure 3 | Room | 50 | | | | | |
| Charge Injection | Q | $C_L = 1\text{ nF}$, $R_{gen} = 0$ $V_{gen} = 0\text{ V}$, See Figure 4 | Room | 30 | | | | | pC |
| Source-Off Capacitance | $C_{S(off)}$ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ V_S , $V_D = 0\text{ V}$ | Room | 14 | | | | | pF |
| Drain-Off Capacitance | $C_{D(off)}$ | | Room | 14 | | | | | |
| Channel-On Capacitance | $C_{D(on)}$ | | Room | 40 | | | | | |
| Input Capacitance | C_{IN} | | $f = 1\text{ MHz}$ | $V_{IN} = 0\text{ V}$ | Room | 6 | | | |
| | | $V_{IN} = 15\text{ V}$ | | Room | 7 | | | | |
| Off-Isolation | OIRR | $V_{IN} = 0\text{ V}$, $R_L = 1\text{ k}\Omega$ | Room | 62 | | | | | dB |
| Crosstalk (Channel-to-Channel) | X_{TALK} | $V_S = 1\text{ V}_{rms}$, $f = 500\text{ kHz}$ | Room | 74 | | | | | |
| Power Supplies | | | | | | | | | |
| Positive Supply Current | I_+ | $V_{IN} = 15\text{ V}$ or 0 V (All Inputs) | Room Full | 0.001 | | 10 100 | | 100 | μA |
| Negative Supply Current | I_- | | Room Full | -0.001 | -10 -100 | | -100 | | |

Notes:

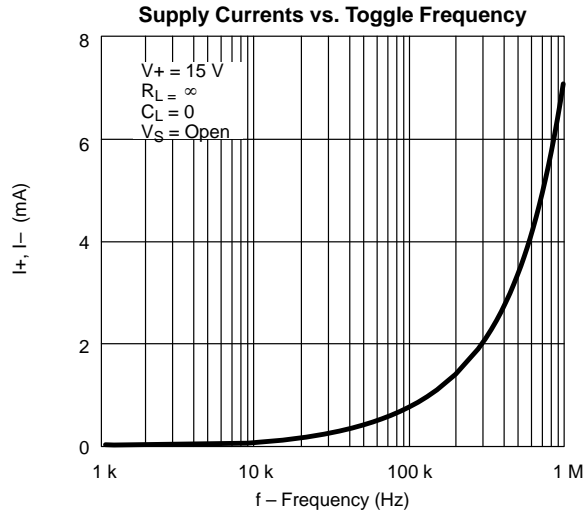
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

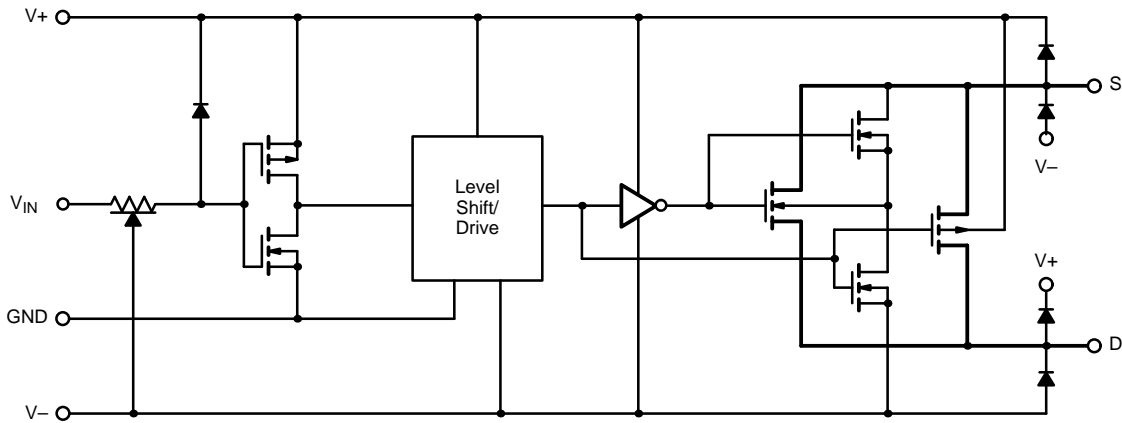


FIGURE 1.

TEST CIRCUITS

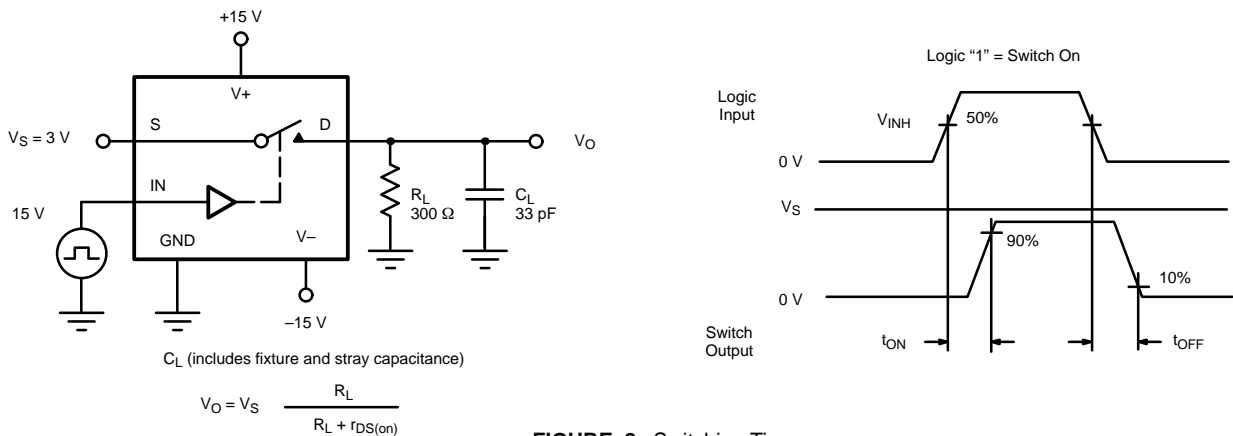
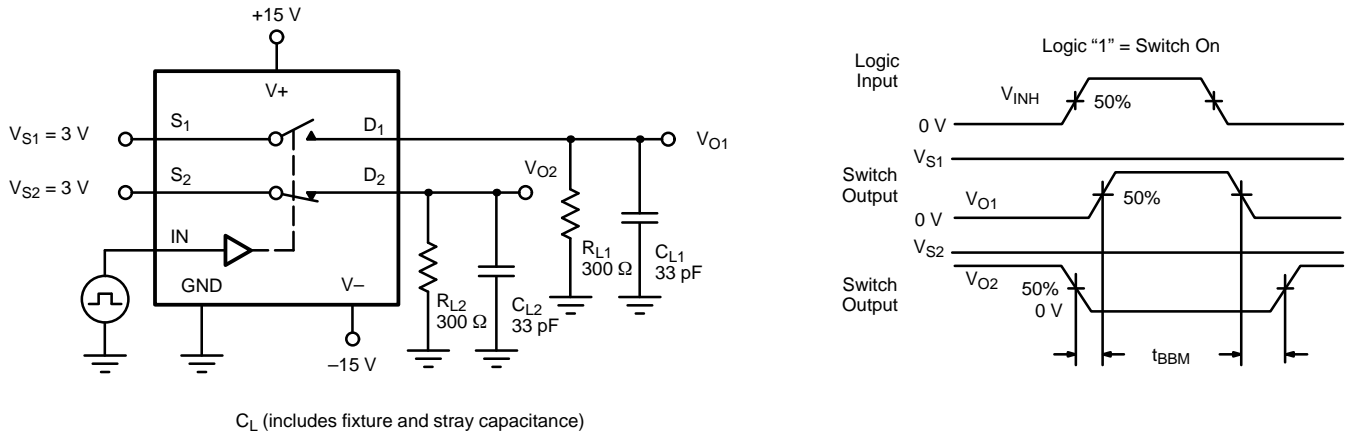
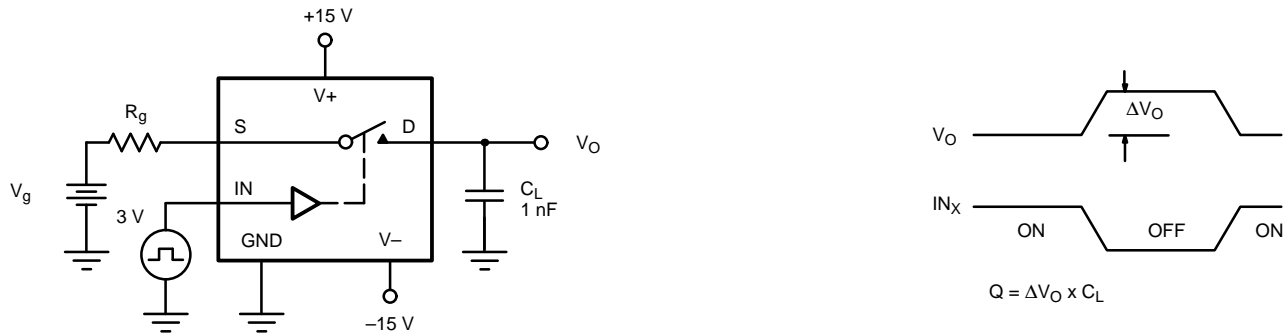


FIGURE 2. Switching Time

TEST CIRCUITS

FIGURE 3. Break-Before-Make SPDT (DG305A, DG307A)

FIGURE 4. Charge Injection

APPLICATION HINTS^a

| V+ Positive Supply Voltage (V) | V- Negative Supply Voltage (V) | GND Voltage (V) | V _{IN} Logic Input Voltage V _{INH(min)} /V _{INL(max)} (V) | V _S or V _D Analog Voltage Range (V) |
|---|---|-----------------------|--|--|
| 15 | -15 | 0 | 11/3.5 | -15 to 15 |
| 20 | -20 | 0 | 11/3.5 | -20 to 20 |
| 15 | 0 | 0 | 11/3.5 | 0 to 15 |

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

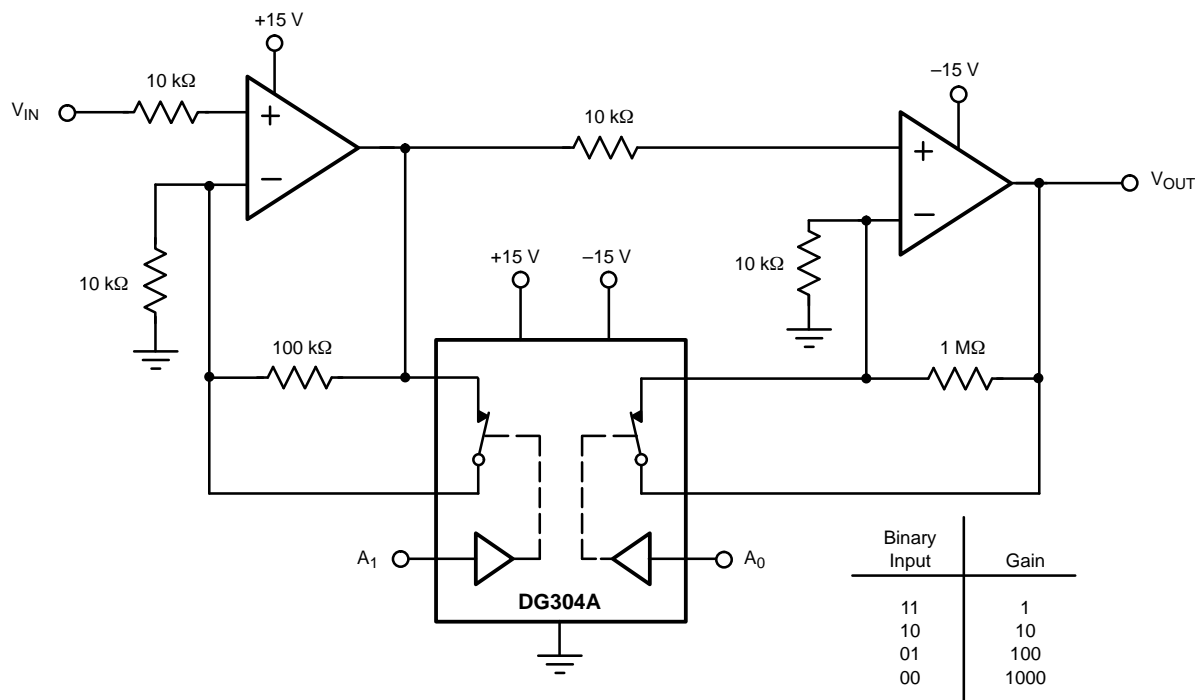


FIGURE 5. Low Power Binary to 10^n Gain Low Frequency Amplifier

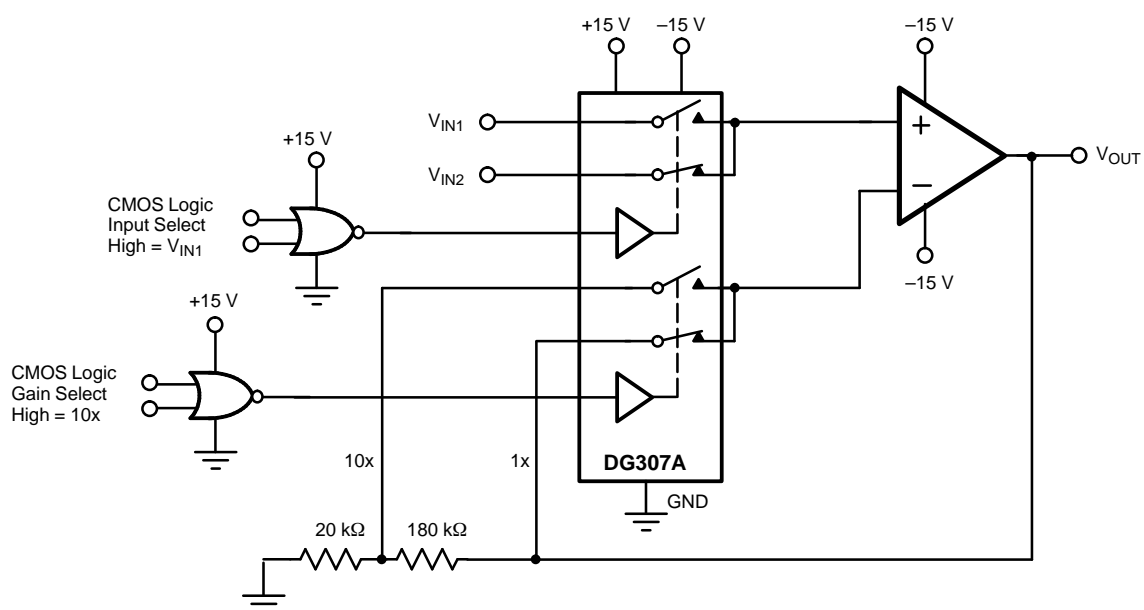


FIGURE 6. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain



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